A New Stacked SMVP(Surrounded Micro Villus Patterning) Cell for 256 Mega and 1 Giga bit DRAMS


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A new capacitor structure called SMVP is proposed. The SMVP capacitor is characterized by enlarged storage node pattern beyond lithographical limit and a surrounding wall around micro villus bars. The measured capacitance of the SMVP structure in 0.72 \( \mu \text{m}^2 \) cell size is 39.3 fF. In addition, the electrical results such as leakage current, breakdown voltage and TDDB of the SMVP structure are proven to be comparable to those of stack structure.

Introduction

To obtain a sufficient storage capacitance in a small cell area of 256Mb DRAM and beyond, an enlargement of effective surface area of capacitor electrode is required\(^{1,2}\). We have demonstrated the MVP capacitor structure for 256Mb DRAM\(^3\). In this paper, we present a SMVP (Surrounded Micro Villus Patterning) process which can achieve even more cell capacitance than that of MVP structure. The major features of SMVP structure are forming surrounding walls around micro villus structure using low temperature processes. Almost 40 fF of cell capacitance is obtained in 0.72 \( \mu \text{m}^2 \) (1.2*0.6) cell size by adopting a new surrounding wall. And a modified (HSG - combined) SMVP structure increases cell capacitance furthermore, which can be extended for 1 Giga bit DRAM cell.

SMVP Fabrication Technology

Fig.1 shows a schematic process sequence of SMVP capacitor structure. A cross-sectional SEM picture of the SMVP structure is shown in Fig. 2. The key process steps of the SMVP structure are as follows. After the development of photo-resist for the storage node patterning, a PE-oxide (200 \(^{3}\)) layer is deposited and etched to form PE-oxide spacer around
the sidewall of the photo-resist pattern. In general, the step-coverage of the low temperature oxide is poor, but using in-situ deposition and etch-back process, the step-coverage of PE-oxide is improved enough to form spacer of 500Å thickness. As a result, the enlarged storage node pattern beyond the lithographical resolution limit is produced by following etching process (in Fig. 1, 'S' denotes spaces between neighboring cells). Thereafter, the photo-resist pattern is stripped off to expose HSG-archipelago pattern and the pattern is transferred to the oxide layer underneath it. And transferred oxide-archipelago pattern and PE-oxide spacer are used as an etch mask to produce villus bars with a surrounding wall using a subsequent etching process. Finally, above oxide masks are stripped off. In Fig. 2, micro villus bars of 0.4μm height and surrounding walls are nicely formed and the spaces between neighboring storage nodes are less than 0.2μm. To obtain 4 nm(Tox.eq) dielectric films, the in-situ nitridation process is applied 4).

Results and Discussion

Fig. 3 shows capacitance voltage characteristics of MVP-based capacitors, including SMVP capacitor. Due to the enlarged surrounding wall, the measured capacitance value for the SMVP structure in 0.72 μm² cell size becomes 39.3 fF(Tox.eq=4nm), which is enough for 256Mb DRAM, even at low operation voltages down to 2.0 V. The reduction of capacitance due to the

Fig. 2 SEM Cross-sectional view of SMVP capacitor

Fig. 4 SEM Cross-sectional view of HSG-combined SMVP capacitor

Fig. 3 C-V characteristics of MVP-based capacitors

Fig. 5 Measured and estimated capacitances trend of SMVP capacitor for 256 Mega and 1 Giga bit DRAMs (height = 0.5μm, Tox.eq = 4nm)
depletion layer of micro villus bars is less than 3% at 3V of cell plate voltage. In Fig. 3, the modified SMVP with small HSG on the surface of the SMVP is expected to have a surface area of 1.5 times larger than that of the SMVP structure. The bird's eye view of the modified SMVP structures is shown in Fig. 4. As shown in Fig. 5, the SMVP structure can be applied into 1 Giga bit DRAM cell. The modified SMVP structure predicts even more high capacitance value (29 ff) for 0.35 µm² cell area (0.42 µm x 0.84 µm) comparing with 19 ff for simple SMVP structure (Tox.eq=4 nm).

Electrical characteristics of SMVP structure with 5.5 nm of NO dielectric thickness show similar breakdown field and leakage characteristics with those of conventional stack structure as shown in Fig. 6(a) & Fig. 7(a). For 4 nm (Tox.eq) of NO dielectric films, the resulting leakage current density shown in Fig. 7(b) stays below the allowable level of 1 fA/µm² at capacitor operating voltage of 1.5 V (both positive and negative biases). Breakdown characteristics of the SMVP structure for Tox.eq=4 nm are shown in Fig. 6(b), which are similar to those of the simple stack cell structure. The expected lifetime at the capacitor operating voltage of 1.5 V far exceeds ten years as shown in Fig. 8.

**Conclusions**

A new capacitor structure called SMVP is proposed. The measured capacitance of the SMVP structure in 0.72 µm² cell size is 39.3 ff. Also, estimated capacitance values for 1 Giga bit DRAM are 19.3 ff with the SMVP and 29 ff with the Modified SMVP, respectively. In addition, the electrical results such as leakage current, breakdown voltage and TDDB of the SMVP structure are proven to be comparable to those of stack structure. Therefore, the SMVP capacitor structure is expected to be the most promising candidate for 256 Mega and 1 Giga bit DRAMs.

**References**