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# A Two-Terminal ($T^2$) Cell for Ultra High Density DRAMs

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In order to realize a small memory cell with an easy-to-make structure, we propose a new Two-Terminal ($T^2$) cell concept. This cell consists of a multilayered N-P-N device acting as a transfer gate and a capacitor storing data. The $T^2$ cell has only two terminals connected to a bit-line and a word-line respectively, while the conventional cell requires four terminals. Because of this simple and unique cell configuration, a cross-point-type cell structure for future ultra high density DRAMs can be easily realized.

## INTRODUCTION

A large variety of conventional one-transistor one-capacitor cells have been studied for higher density DRAMs. For megabit DRAMs, innovations are chiefly focused on the 3-dimensional capacitor structure to realize sufficient storage capacitance. Consequently, many kinds of trench or stacked capacitor cells are reported. Furthermore, for the gigabit DRAM cells, the transistor also becomes an object of innovations. Cross-point-type cells with a vertical transistor are proposed[1][2]. However, the structures of these cross-point-type cells are complicated and requires very complicated processing steps.

In order to overcome this problem, we propose a new Two-Terminal ($T^2$) Cell concept for future ultra high density DRAMs. The $T^2$ cell has a simple and unique configuration with only two terminals. Therefore, it results in a small cross-point-type cell with an easi-to-make structure.

## CELL CONCEPT

The $T^2$ cell is composed of two elements, a two-terminal switch and a capacitor. We adopted a multilayered N-P-N device for the two-terminal switch.

Figure 1(a) shows the equivalent circuit of the $T^2$ cell. The multilayered N-P-N device has Symmetrical and Bi-directional Switching (SBS) I-V characteristics. It is connected between a bit-line (BL) and a storage node (SN), acting as a cell transfer gate. Furthermore,

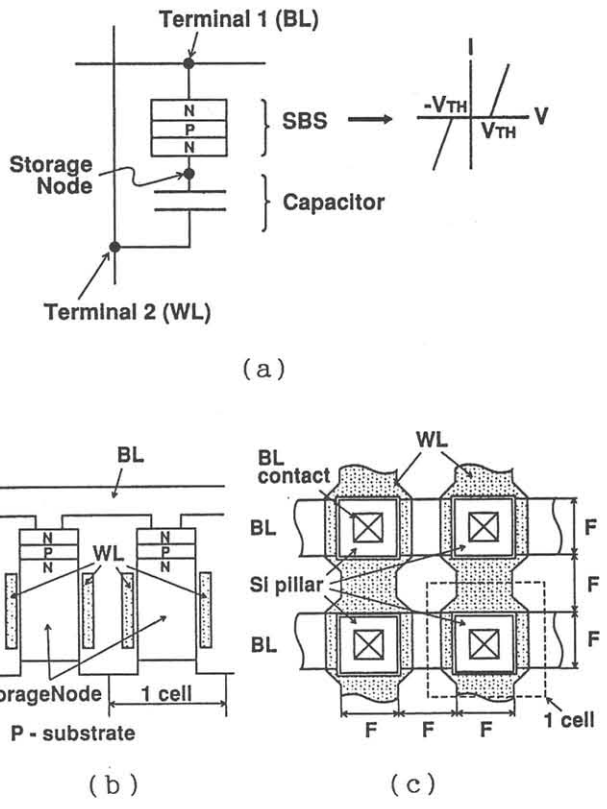



**Fig.1** (a) Equivalent circuit and SBS I-V characteristics, (b) cross-sectional view normal to WL deriction, and (c) top view of $T^2$ cell. F is the minimum feature size.

a capacitor is connected between the SN and a word-line (WL). As a result, the $T^2$ cell has only two terminals connected to the BL and the WL respectively, while the conventional cell requires four terminals. Due to this simple and unique cell configuration, the $T^2$ cell is suitable for the cross-point-type structure.

Figure 1(b)(c) show the cross-sectional view normal to WL direction, and the top view of the cross-point-type $T^2$ cell. The minimum cell size of $4F^2$ (F:feature size) is obtained with the relatively simple and easy-to-make structure.

## OPERATION

The write/read operation of the $T^2$ cell is performed as follows (Fig.2). In the write mode of a logical "1", $V_{CC}$ is applied to the BL, and the selected WL is grounded. Since the SN voltage ($V_{SN}$) is also lowered by the coupling with the selected WL, the voltage difference between the BL voltage ($V_{BL}=V_{CC}$) and $V_{SN}$ is increased. This voltage difference is larger than the threshold voltage ($V_{TH}$) of the SBS device and causes a write current ($I_{write}$) to flow from the BL to the SN (Fig.2(a)). Thus the capacitor is charged and a "1" is written. In the read mode of a logical "1", after the BL is precharged to $V_{CC}/2$, $V_{WL}$ is raised. Contrary to the write mode, $V_{SN}$ becomes higher than $V_{BL}$ ($=V_{CC}/2$). As a result, a read current ($I_{read}$) flows in the direction opposite to $I_{write}$ (Fig.2(b)). Thus, electric charge stored in the capacitor is transferred to the BL. By amplifying the $V_{BL}$ change, the read operation is carried out in a similar way as the conventional sensing method. Thereafter, the restore operation can be performed by lowering $V_{WL}$ as in the write operation.

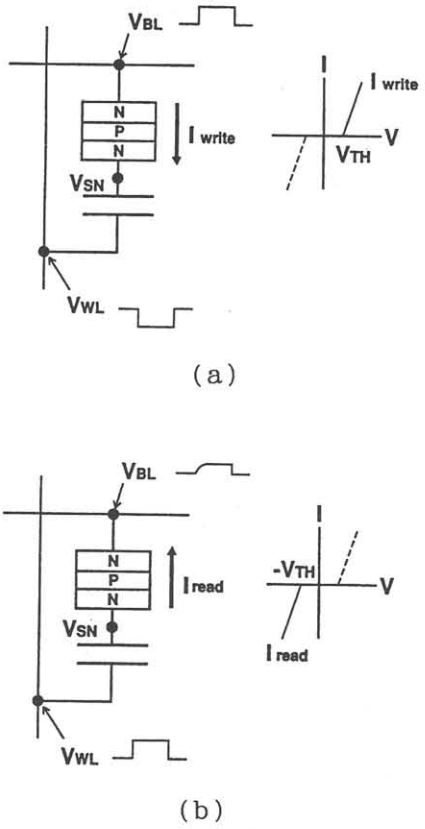
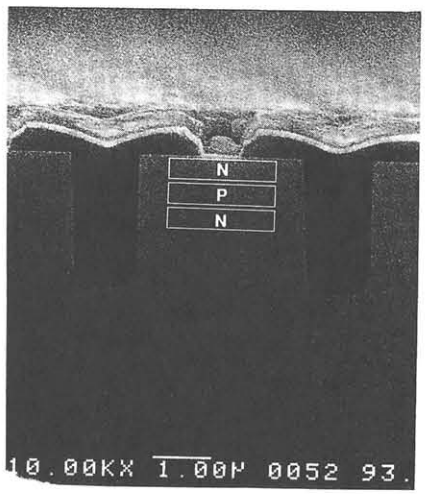
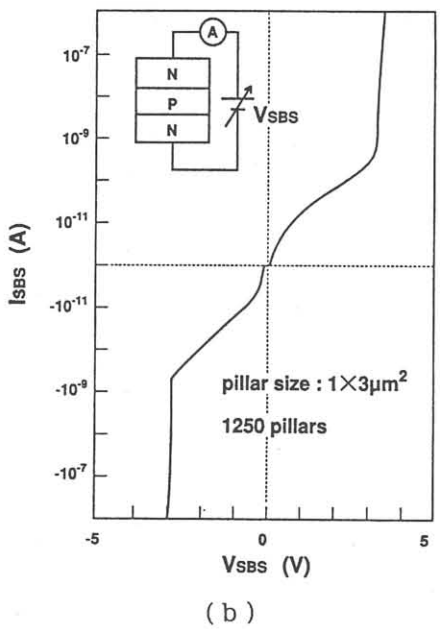



**Fig.2** (a) "1" writing operation, and (b) "1" reading operation of $T^2$ cell.




(a)




(b)

**Fig.3** (a) Cross-sectional SEM photograph, and (b) SBS I-V characteristics of vertical N-P-N device.

In the write mode of a logical "0", the BL is grounded and $V_{CC}$ is applied to the selected WL, contrary to that for a logical "1". Thus, the capacitor is charged in the polarity opposite to that for a logical "1" and a "0" is written. Therefore, no electric charge is transferred to the BL, even if $V_{WL}$ is raised for the read operation.

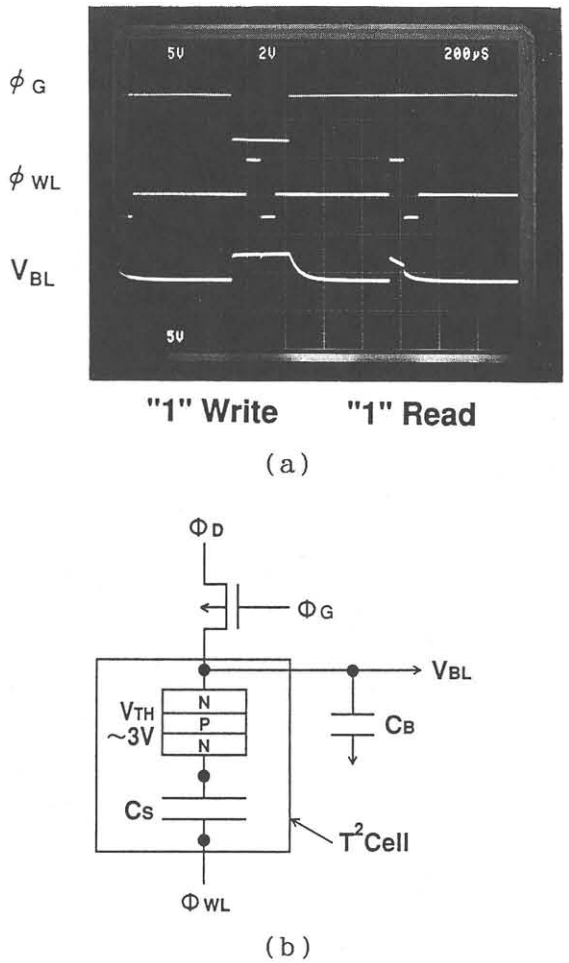



**Fig.4** (a) Operating waveforms in a sequence of "1" writing and "1" reading, and (b) schematic of the test circuit for $T^2$ cell.

## RESULT and DISCUSSION

We have fabricated a vertical N-P-N device which is a key element for the cross-point-type cell structure (Fig.3(a)). In order to realize the SBS I-V characteristics, the same doping profiles are required for the two P-N junctions of the N-P-N device. To obtain the symmetrical N-P-N doping profile, ion implantation has been used. SBS I-V characteristics with a low subthreshold leakage current are achieved (Fig.3(b)).

We confirmed the write/read cell operation by a test circuit (Fig.4).

The cross-point-type $T^2$ cell has a similar structure as the SGT cell proposed for conventional high density DRAMs[2]. In comparison with the SGT cell (Fig.5), the $T^2$ cell has several advantages.

(1)In the SGT cell, 2 poly silicon layers are used, one for the cell plate and one for the WL, resulting in very difficult processing steps. The $T^2$ cell requires only 1 poly silicon layer.

(2)Difficult $V_{TH}$ control for the vertical transistor is not required.

(3)Because the $T^2$ cell in principle does not need a substrate bias, the P-substrate can be replaced with $SiO_2$. This SOI-structure would realize superior soft error immunity.

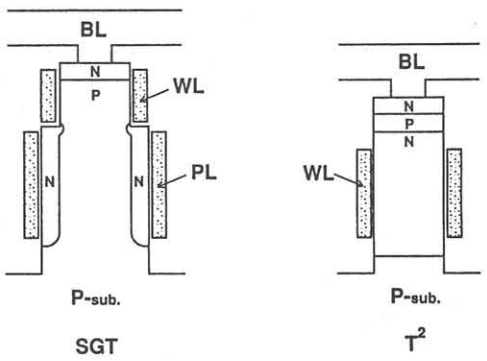



**Fig.5** Comparison of memory cell structure between $T^2$ cell and conventional SGT cell.

## CONCLUSION

The Two-Terminal ($T^2$) cell concept has been proposed and the functionality is demonstrated. Due to the simple cell configuration, it is extremely attractive for application in future ultra high density DRAMs.

## ACKNOWLEDGMENT

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