Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 856-858

Electrical Characterization of RTN-Poly-Si/CVD-Ta_2O_5/CVD-TiN Stacked DRAM Capacitors

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The integration of RTN-poly-Si/CVD Ta_2O_5/CVD TiN capacitors has been investigated for three dimensional DRAM structures. The effect of annealing conditions after Ta_2O_5 deposition and also after top electrode (TiN) deposition on the dielectric characteristics has been examined for rapid thermal and furnace processing. Rapid thermal annealing above 800°C after capacitor formation (post TiN deposition) resulted in a significant degradation of the leakage characteristics without any change in the capacitance. This will be an important factor in the successful integration of these structures.

1. INTRODUCTION

The manufacture of DRAMs beyond 64 Mbit requires the development and integration of advanced capacitor dielectric materials to achieve the level of capacitance needed for reliable device operation without severely complicating the capacitor structure. The high dielectric constant (> 20) of tantalum penta oxide (Ta_2O_5) offers a potential alternative to the silicon nitride films conventionally used in DRAM capacitors. However, the introduction of Ta_2O_5 in DRAMs has not been very effective due to the continuing improvements in the structural and electrical characteristics of silicon nitride films [1-4], the development of textured capacitor structures [5], and the high leakage current originally observed in these films. The leakage current can be reduced to acceptable levels by a combination of annealing steps [6] and recent work has shown that it can be further lowered by reducing the carbon content in the film [7]. From an integration standpoint, work on RTN-Poly-Si/Ta_2O_5/TiN capacitors have demonstrated capacitance values as high as 13.8 fF/μm^2 [8] on smooth electrodes and 20.4 fF/μm^2 [9] on HSG-Si storage nodes, while satisfying the leakage current and lifetime requirements for DRAMs. However, most of this work has been based on the use of sputtered TiN top electrodes, while for three dimensional (3D) structures it is critical to have a chemical vapor deposition process for the top electrode. In this paper we report on the electrical properties of 3D stacked capacitors formed with CVD-Ta_2O_5 and CVD-TiN and also examine the effect of anneal treatments performed after Ta_2O_5 and after TiN (top electrode) deposition.

2. EXPERIMENTAL

Three dimensional capacitor structures (Fig. 1) were fabricated on n-type silicon substrates with a 200nm SiO_2 layer.

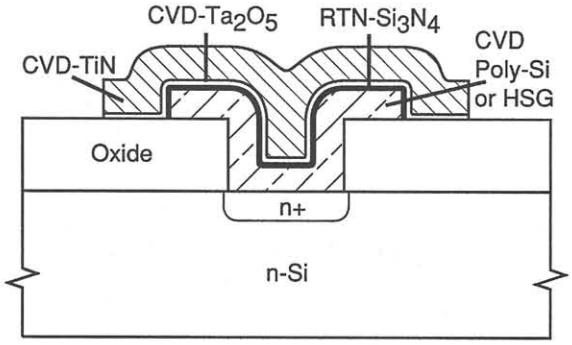


Fig. 1. Section of the 3D capacitor structure. A successful integration requires all layers to be grown by CVD.

The bottom electrode of the capacitor was accessed through the substrate. The 120 nm phosphorus doped bottom electrode consisted of either smooth polysilicon or HSG (rugged) silicon LPCVD films [9]. The polysilicon films were subjected to rapid thermal nitridation (RTN) in NH_3 at 950°C for 30s to prevent the formation of interfacial silicon dioxide. 10nm and 15nm Ta_2O_5 films were deposited by LPCVD at 350°C or 400°C using $Ta(OC_2H_5)_5$ and O_2. These films were annealed under various conditions (ambient, temperature, time) in a furnace or rapid thermal processor. The top TiN electrode was deposited using CVD [10] and patterned to form the capacitor structure. The final capacitor structure was also subjected to rapid thermal annealing at different temperatures. Capacitance-voltage (CV) and current-voltage (IV) measurements were done on 412μm^2 structures to determine the capacitance and leakage characteristics.

3. RESULTS AND DISCUSSION

The effect of rapid thermal processing after Ta_2O_5

Fig. 2. Effect of post Ta_2O_5 rapid thermal processing on the voltage to induce 1 $\mu A/cm^2$ (V_{crit}) and capacitance for (a) rugged and (b) smooth polysilicon electrodes.

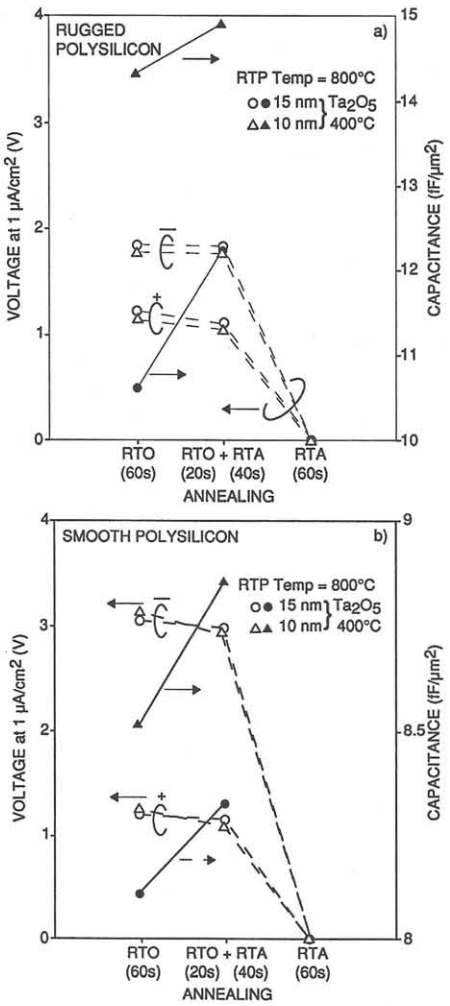
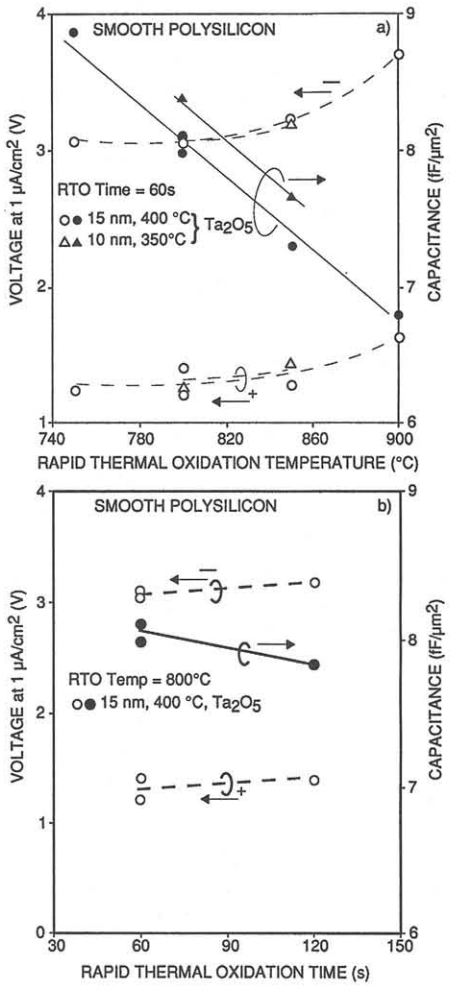


Fig. 3. Effect of post Ta_2O_5 RTO (a) temperature and (b) time on V_{crit} and capacitance.



deposition on the capacitance and voltage for a leakage current of 1$\mu A/cm^2$ (V_{crit}) is shown in Fig. 2 for rugged and smooth polysilicon electrodes. The three different annealing conditions consisted of rapid thermal annealing (RTA) at 800°C for 60s; RTA at 800°C for 40s with rapid thermal oxidation (RTO) at 800°C for 20s; and RTO only at 800°C for 60s. The importance of the oxidation component is clearly demonstrated in the leakage characteristics. Increasing the extent of RTO does not significantly lower the leakage, but it sharply reduces the capacitance. The thickness of the Ta_2O_5 film does not have a strong effect on the leakage behavior. The larger percentage increase in capacitance for the rugged polysilicon electrode when the film thickness is reduced, when compared to the smooth polysilicon electrode, is due to the absence of Ta_2O_5 bridging between the HSG grains for the thinner film [11]. There is a linear decrease in the capacitance with an increase in RTO temperature at 60s (Fig. 3a). However, the leakage current is almost constant up to 850°C, beyond which it shows a sharper decrease. The capacitance for the 350°C Ta_2O_5 film is slightly higher but it shows similar leakage characteristics. The higher capacitance could be due to the variation in the film thickness and, as observed earlier, should not have a strong effect on the leakage behavior. Increasing the RTO time (Fig. 3b) at 800°C reduces the capacitance and the leakage current.

From the above observations, the lowest RTO temperature (750°C) and time (60s) gave the highest capacitance. Further increase in the RTO temperature or time does not significantly reduce the leakage current, but it drastically lowers the capacitance. These changes can be associated with the formation of a silicon dioxide layer at the Ta_2O_5/polysilicon interface. A thicker SiO_2 layer reduces the leakage current and the capacitance.

The effect of adding a nitrogen or oxygen furnace anneal for 30 minutes at various temperatures to the RTO (800°C/60s) process is shown in Figs. 4a and b. The additional nitrogen anneal results in a sharp drop in the capacitance between 700°C and 800°C, then remains relatively stable at higher temperatures. There is very little change in the leakage current. The added oxygen anneal results in a decrease in capacitance as well as the leakage current.

The additional anneals did not result in further gains (capacitance x V_{crit}) to the RTO process. Annealing in nitrogen can lead to the crystallization [12] of the film as well as shrinkage due to the desorption of CH_4 and O_2 [13]. The corresponding changes in the leakage current could be due to the reduction in the thickness of the dielectric or the formation of grain boundaries/grooves on the surface [14]. The changes with the oxygen anneals are caused by the formation of the interfacial oxide.

The effect of rapid thermal annealing for 20s at various temperatures after the TiN electrode formation is shown in Fig. 5. All the samples were subjected to an 800°C/

Fig. 4. Effect of post Ta_2O_5 furnace annealing on (a) capacitance and (b) V_{crit}.

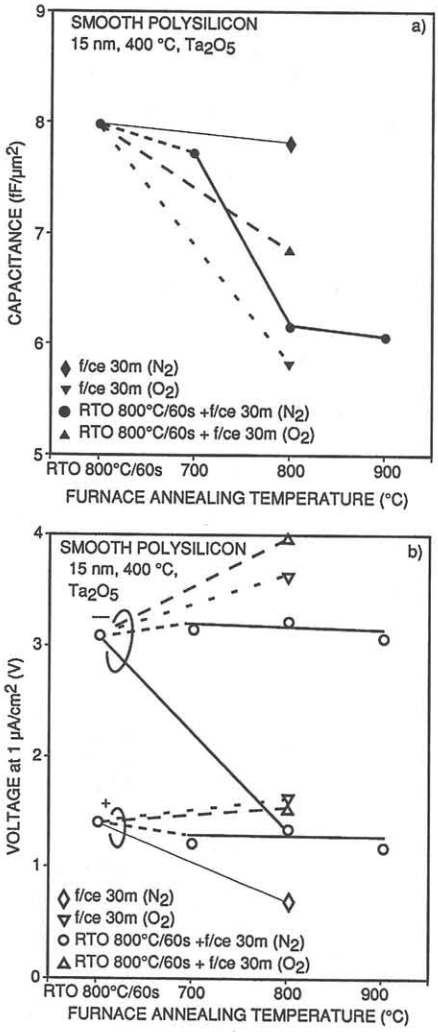
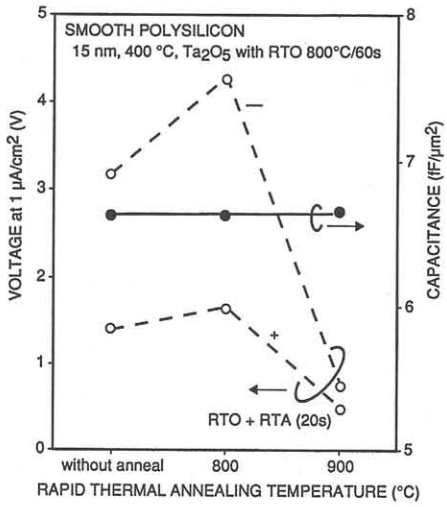


Fig. 5. Changes in V_{crit} and capacitance with annealing after capacitor formation (post TiN deposition).



60s RTO after Ta_2O_5 deposition. The capacitance is not at all affected by the anneal, but there is drastic increase in the leakage current at 900°C. This is believed to be caused by the interaction between the TiN electrode and Ta_2O_5. The higher affinity of oxygen to titanium than tantalum leads to the reaction of the metallic Ti with the oxygen at the surface of the Ta_2O_5 layer. This depletes the oxygen in the Ta_2O_5 film and results in the generation of oxygen vacancies which are responsible for degradation in the leakage behavior [15]. This could be a limiting factor in the integration of these structures when post capacitor processing temperatures exceed 800°C.

4. CONCLUSIONS

The integration of Ta_2O_5 dielectric films for 3D DRAM structures was investigated using CVD TiN top electrode. Rapid thermal oxidation without any additional anneals can be used to reduce the leakage current without effecting the capacitance. The capacitor structures without any post top electrode annealing exhibits dielectric characteristics that are comparable to sputtered top electrodes. However, a severe degradation in leakage characteristics is observed when the capacitor structures are annealed above 800°C and will have to be taken into consideration for DRAM integration.

ACKNOWLEDGMENTS

The authors would like to thank the Process Development and Manufacturing groups for the fabrication of the devices and Brenda Jameson for assistance in the preparation of the manuscript.

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