

Invited

DRAM Technology for Giga-bit Age

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This paper discusses a memory cell technology, a low power and low noise circuit technology and a systematization DRAM technology for realizing Giga-bit DRAMs, which are predicted to be practically used in year 2000. It is concluded that a planar-type memory cell with an extremely high ϵ film capacitor, a multi-divided cell array structure and a DRAM with CPU architecture are promising as key technologies for future Gb DRAMs.

1. INTRODUCTION

Since the first 1Kb DRAM was developed in 1970, DRAMs have always progressed in the highest bit density as a leader in LSI technology development. Already, 256 Mb DRAMs with 0.25 μ m feature size have been developed [1,2] and Gbit DRAM technology development race has started. Figure 1 shows trends in feature size (F), cell size (Sc), chip size, N value ($Sc = NF^2$), supply voltage (Vcc) and access time for DRAM generations from 1Mb. According to these trends, 0.15-0.18 μ m and 0.1-0.12 μ m feature sizes are predicted for 1Gb and 4Gb DRAMs, respectively. In order to overcome a crisis in too expensive production costs, Gb DRAMs with those fine patterns strongly require a process and device technology targeting an easy-to-make, low cost and high yield feature, and a circuit and architecture technology with low power, low noise and wide operation margin. In addition, from Gb DRAM application viewpoints, systematization DRAM technology to attain high I/O bandwidth to CPU will become increasingly important.

2. MEMORY CELL TECHNOLOGY

The main problem in developing Gb DRAMs is related to the scaled-down memory cell technology. Figure 2 shows a trend in 1-transistor and 1-capacitor (1-T) cell structures developed since 1Mb DRAMs. Simple planar capacitors which used up to 1Mb, were replaced by three dimensional (3-D) stacked/trench capacitors in 1Mb/4Mb DRAM generations, where the capacitance is 2-3 times larger than that of the planar capacitor. In 64Mb/256Mb DRAM generations, more complicated

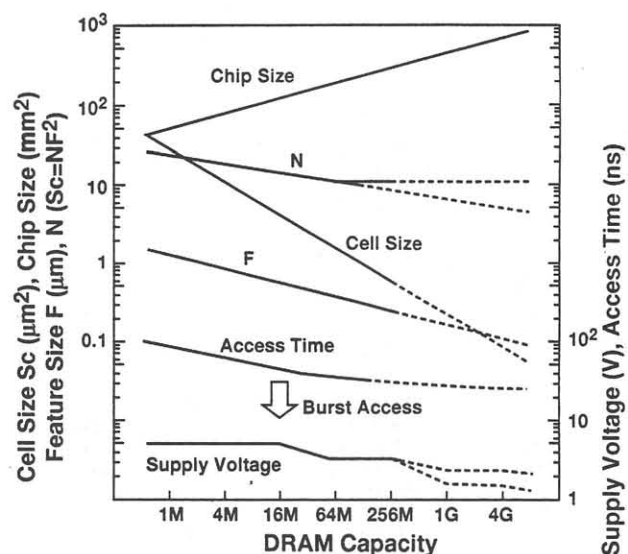


Fig.1 DRAM feature trend.

3-D stacked and trench capacitors have been proposed and developed. In Gb DRAMs, however, the complexity of those capacitor structures with 30fF storage capacitance (C_s) becomes too crucial to keep reasonable production cost and yield. Therefore, the simple planar-type capacitor with sufficient C_s is essential. One solution would be to apply an extremely high ϵ dielectric film layer to such a simple capacitor. Ferroelectric materials, such as BaSrTiO₃ film with less than 100nm thickness, are promising candidates for Gb DRAM cell capacitors [3], as shown in Fig.3.

Bit-line sense signal(V_s) from the 1-T cell is proportional to $V_{cc}/2(1+C_b/C_s)$, where C_b is bit-line capacitance. For increasing V_s , reducing C_b is as important as increasing C_s . C_b can be reduced by adopting trench isolation or SOI structure in the cell transistor. The junction capacitance in the trench isolation decreases to about half of that in the LOCOS isolation [4]. The SOI transistor also has advantages in small C_b and α -particle immunity, but the leakage current and process cost should be reduced.

Relaxation in feature size, as well as miniaturization in cell size, contribute to high yield and wide operation margin for Gb DRAMs. The cell size of 256Mb DRAMs including process margin, has already shrunk down to $10F^2$. A further reduced N value is necessary for Gb DRAM cells. The conventional cell in the folded bit-line structure needs $8F^2$ as a minimum cell size, neglecting the process margin. However, the cell size can be reduced by using the open bit-line cell, $6F^2$, or the BORAM cell, $4F^2$ [5,6]. They can be candidates for Gb DRAM cells, but the circuit technology to maintain the cell operation margin at the same level as the folded bit-line cell should be developed.

3. LOW POWER/NOISE CIRCUIT TECHNOLOGY

The chip size of Gb DRAMs will be more than $450mm^2$, which causes serious degradations in operation margin due to increased wiring length in both signal and power lines; 1) increased signal delay due to wiring resistance, 2) increased cross-talk noise between signal lines, and 3) increased power line voltage bounce. These degradations can be overcome by reducing the cell array activation size and adopting hierarchical world-line and data-line structures. The former technique reduces not only the active current but also the peak operating current, which suppresses the power line voltage bounce, resulting in higher operation speed. The latter technique relaxes the layout pitch of main word-lines and data-lines, which reduces the wiring resistance, the inter-wiring capacitance and the cross-talk noise, resulting in higher speed and wider operation margin. These techniques are realized by a multi-divided cell array structure combined with dual word-line and non-multiplexed address input schemes [1], which can reduce the active cell array size down to an arbitrary size. Figure 4 shows sensing waveforms and power line voltage bounces for 1/32 and 1/1024 partially active cell array sizes in the 256Mb DRAM. As both the active current and the peak operating current decrease due to reduced active cell array size, power

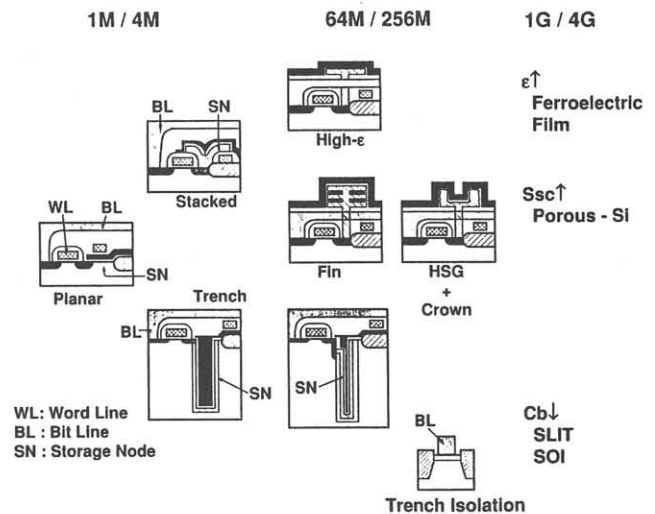


Fig.2 1-T cell structure trend.

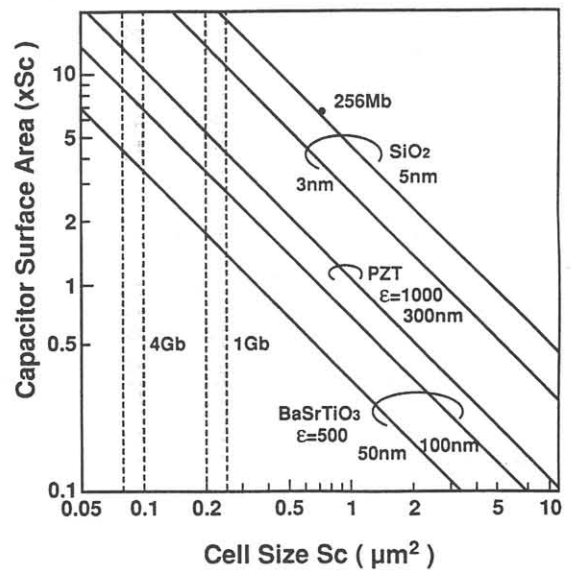


Fig.3 Relations between cell size and capacitor surface area to obtain 30fF C_s .

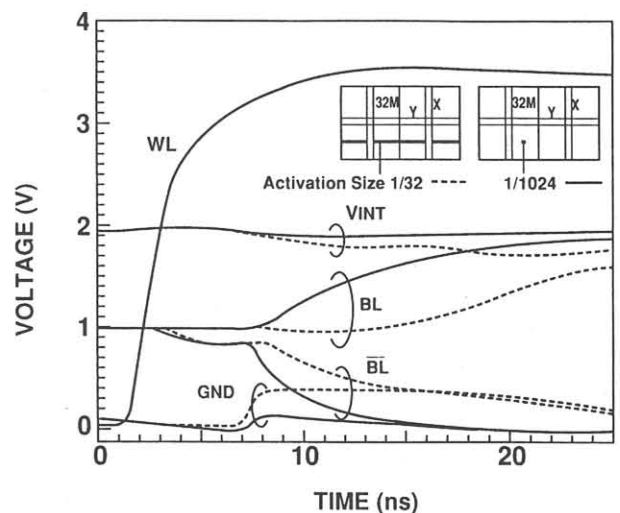


Fig.4 Sensing waveforms and power line voltage bounces in the 256Mb DRAM.

line voltage bounces are also suppressed, leading to higher speed sensing. Applying these techniques to cell arrays of 1Gb and 4Gb DRAMs, 1/4096 and 1/16384 partial cell array activation, respectively, can maintain the operating current at the same negligible level as that of the 256Mb DRAM, as shown in Fig.5. Conventional refresh cycle trend, 32K for 1Gb and 64K for 4Gb, is kept by refreshing the divided cell arrays, distributively and serially at one refresh cycle.

Battery operation is a clear target for Gb DRAM design requirements. Low voltage operation directly leads to low power for the battery operation. But, bit-line sense signal V_s decreases due to reduced high storage voltage, resulting in lower operation margin. The partial cell array activation technique can minimize the power dissipation as well as preserving V_s from the cell at maximum, in spite of using the maximum V_{cc} to ensure the cell reliability. It is the most promising technique to attain low power and low noise operation for Gb DRAMs.

4. SYSTEMATIZATION DRAM TECHNOLOGY

The progress in DRAM performance has been focused on the data transfer rate from/to CPU. The rate increases by large I/O bit width and high speed I/O operation, as shown in Fig.6. High speed DRAMs, such as synchronous DRAM (SDRAM) [7,8], Rambus DRAM [9] and cache DRAM [10], can transfer I/O data at more than 100MHz rate, synchronously with a system clock. However, in order to speed up the data transfer rate of these DRAMs, the I/O interface from/to CPU causes a bottleneck. Although many high speed I/O interfaces are proposed [11], it is very difficult to increase both the interface speed and the I/O bit width up to more than 500-MByte/s and 64bits. A solution is to integrate CPU on the DRAM chip, which can achieve an extremely high data transfer rate between DRAM and CPU by means of large I/O bit width, for example, 1K I/O bits. Since such a chip integrates a Gb DRAM and CPU, the required DRAM technology should be capable of implementing high speed logic circuits.

5. CONCLUSION

For realizing Gb DRAMs with sub-quarter μm feature size, the planar-type memory cell with high ϵ film capacitor should be developed. From circuit and system viewpoints, the multi-divided cell array structure and the DRAM with CPU architecture will be promising techniques for future Gb DRAMs.

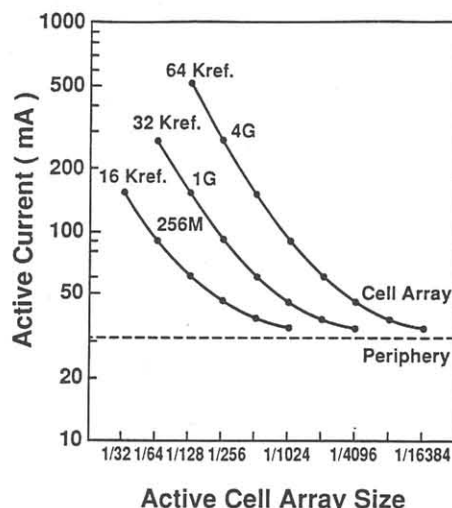


Fig.5 Active current reduction by partial cell array activation techniques.

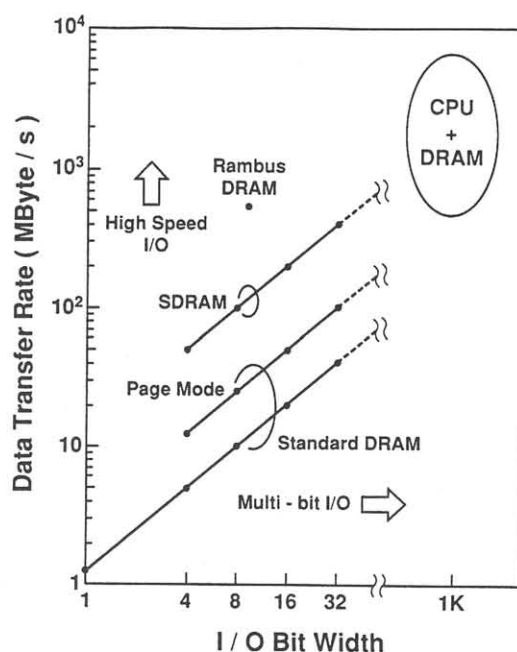


Fig.6 Development trend in data transfer rate of high speed DRAMs.

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