Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 339-340

Invited

Single Electrons: Status and Prospects

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Single electronics may have a relevant potential for future nanoscale electronic circuits. Some problems will have to be solved: much smaller junctions will have to be fabricated; random offset charges must be eliminated or circumvented; i/f and telegraph noise eliminated. The potential parameters, if succesful, are discussed.

In single electronics, electrons are manipulated one by one, by means of the Coulomb charging energy that is associated with their presence or absence. One needs structures with very small capacitance, so that the energy $e^2/2C$ is significant with respect to the thermal energy. One also needs tunnel junctions with very high resistances, to ensure that the charge is well-localized on a certain conducting island and can only travel to and from it in a discrete event. Single electronics moved from a theoretical concept, mainly associated with transport in granular materials with very small grains, to a controlled phenomenon in fabricated circuits. In the last five years metallic tunnel junctions and semi-conducting nanostructures with capacitances below 10^{-15} F were made; in these circuits of two or more junctions clear results on charging effects were obtained. Using capacitive gates the "Coulomb blockade" can be suppressed and in this way first transistor like devices were obtained. A capacitance of 10^{-15} F corresponds to a charging energy of 80 meV or a temperature of 0.9 K. To see the effects, these devices are cooled in a dilution refrigerator to below 100 mK.

Now that the principle of their functioning has been proven, it is reasonable to ask what is possible with such devices, in particular when future fabrication techniques will allow fabrication of much smaller devices. In a limited number of groups serious attempts are undertaken to improve the technology and to investigate the functioning of devices and circuits. In this paper the status is reviewed with emphasis on the problems that have to be overcome. The limits of what may be achieved in future, given ideal fabrication methods, will be discussed as well.

One of the most important issues is the reduction of the capacitance, in order to achieve a shorter response time as well as a higher operating temperature. Present metallic junctions are about 100x100 nm^2, made of aluminum with aluminum oxide barrier. A shadow evaporation method is employed with in situ oxidation. It should be possible to reduce the size of the junctions down to 30x30 nm^2 with the same method. This will decrease the capacitance by a factor 10 with a corresponding increase of the charging energy. Further improvement will be achieved by fabrication of co-planar electrodes where tunneling is through a lower semiconducting barrier. It is expected that capacitances will go down to 10^{-17} F in this way. Similar improvements are possible with the semiconductor quantum dot circuits. Here the charge-receiving island is defined in a two-dimensional electron gas, usually in a GaAs/AlGaAs heterostructure, by metallic gates.

A major difficulty and serious worry for single electronics are the random offset charges. On measuring on a cooled-down sample one usually finds that the minimum conductance is not obtained for zero gate voltage as it should, but at some offset value. This is due to offset charges that are induced by charged impurities around the "island". No systematic study has been performed yet. It may be necessary to design circuits where the functioning is guaranteed even if offset charges are present. Certainly the sudden changes of offset charges will have to be suppressed. They sometimes lead to telegraph noise in the output that prohibits the tuning of a device. Also excessive 1/f noise is sometimes found.

What should eventually be possible with single electronics? If the technological problems are overcome, the capacitances will decrease from 10^{-15} F to 10^{-16} F and 10^{-17} F. Eventually, nanofabrication on a scale of a few nm may yield capacitances of 10^{-18} F. No further reduction is possible before the atomic level is reached. Response times of circuits are given by R_tC, the tunnel resistance times the capacitance. If R_t is low, quantum leakage occurs. Tunneling events take place that invol-

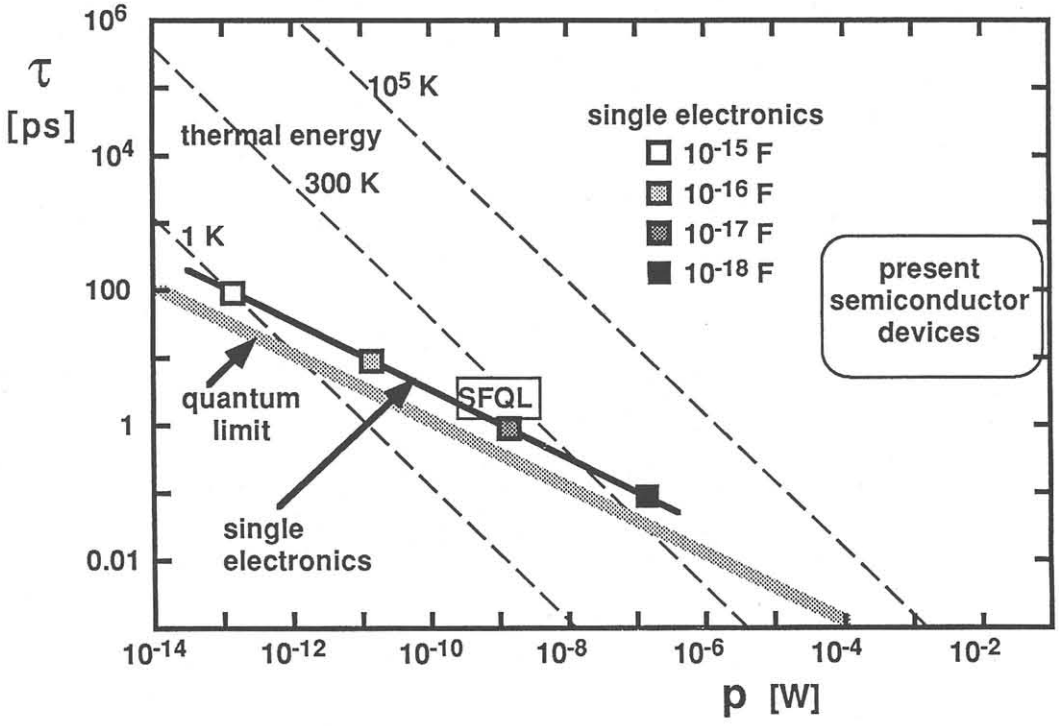

Fig. 1 Switching time versus switching power for single electronics circuits with capacitances varying from 10^{-15} F to 10^{-18} F. SFQL refers to single flux quantum logic with superconducting junctions.

ve multiple junctions. They cannot be controlled. To suppress quantum leakage, R_t has to be much larger than the quantum resistance $\hbar/e^2$, equal to 5 kΩ. A typical value is 100 kΩ, lower is impossible for well-defined operation. This means that response times will decrease from 100 ps for 10^{-15} F to 10 ps (for 10^{-16} F), 1 ps (for 10^{-17} F) and even 0.1 is (for 10^{-18} F). However, the power for switching will increase. That power is the charging energy $e^2/2C$, divided by the switching time R_tC. As the charging energy increases, so does the power $e^2/2R_tC^2$. In figure 1 the time-power diagram is illustrated and compared with other devices. The expected numbers for different capacities are plotted. In the figure the quantum limit is also indicated. A device with switching energy E cannot be operated faster than $\hbar/E$ because otherwise the Heisenberg-uncertainty-given fluctuations in energy exceeds E. This means that the switching power associated with a switching time τ is minimally $\hbar/\tau^2$. That relation is plotted in the figure. Single electron devices actually operate very close to the quantum limit. If $R_t = A(\hbar/e^2)$ where A is between 10 and 100, the switching time is ($\tau = A(\hbar/e^2)C$. The switching power is $E_c/\tau = e^2/2C\tau = (A/2)\ (\hbar/\tau^2)$. For R_t = 100 kΩ, A is equal to about 25.

Single-electron devices can have a significant gain, possibly as high as 1000. Such values have not yet been realized in practical circuits.