Magnetic Flux and Gate Voltage Modulation of the Current in Superconducting Loop of Single Electron Transistors

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The relation between Josephson junctions and superconducting single charge junctions which have ultra-small capacitance (~0.5fF) can be understood by the quantum mechanical conjugate between flux (Φ) and charge (Q). We have fabricated superconducting loop with superconducting single charge transistors and measured its current-voltage (I-V) characteristics at low temperature (~50mK). In this geometry we find that both magnetic flux Φ , and gate voltage V_g , modulate the I-V curve, which shows the superconducting phase coherence exists to some extent in our device.

1. INTRODUCTION

Two small capacitance tunnel junctions connected in series with a capacitively coupled gate, which is so called Capacitively coupled Single Electron Tunneling (C-SET) transistor, display a Coulomb blockade of tunneling due to the small capacitance of the central electrode. In order for electrons to tunnel, a changing energy $E_{\rm C}=e^2/2C_{\Sigma}$ must be paid, where C_{Σ} is the sum of all capacitances between the central electrode and external electrodes. If the central electrode is small enough, then $C_{\Sigma} \approx C_1 + C_2 + C_g$ where C_1 and C_2 are the tunnel junction capacitances, and Cg is the capacitance to one external gate electrode. The coulomb blockade will appear if the temperature is such that $E_{\rm C} >> k_{\rm B}T$. Furthermore, the time for the discharge of this capacitance $\tau = R_n C_{\Sigma}$, where R_n is the tunnel resistance, must be long enough so that the energy uncertainty of the charged state is less than the charging energy, $\hbar/\tau < E_{\rm C}$. This later condition leads to restriction on the tunneling resistance $R_n > R_O$ where R_0 is the quantum resistance, $R_0 = \pi \hbar/2e^2 \approx 6.45 \mathrm{k}\Omega$.

If the tunnel junctions are superconducting state, we normally considered the Josephson coupling energy E_J , which is a measure of the strength of Cooper pair tunneling. This phase coherent process, where charge is transported across the tunnel junction without dissipation of energy, gives rise to the usual Josephson effect. Nevertheless, in the small capacitance Josephson junctions, the charging energy of the Cooper pair $(2e)^2/2C_{\Sigma}$, must also be considered and a finite voltage is required to pass Cooper pairs through the two tunnel junctions. The energy supplied by the voltage source must be dissipated which can be accomplished by two process, exciting modes of the electrodynamic environment, or the tunneling of single electrons (quasiparticles)³).

This device shows a rich structure of I - Vcharacteristics. There are peaks in the current at various bias voltages 1,2) which have been associated with combined Cooper pair and quasiparticle tunneling events^{1,3)}, as well as a resonant tunneling of Cooper pairs 3). Furthermore, the I-V curve can be modulated with an external gate voltage (V_g) via gate capacitance (C_g) . The fundamental period of gate modulation is e/C_g (in some cases $2e/C_g$) arising from a fixed number of electrons (Cooper pairs) on the central electrode. Fixing the number necessarily disrupts the phase coherence, and thus no supercurrent is expected in such a device. In spite of this lack of a zero-voltage current, our experiments show that phase coherence exists to some extent in the Superconducting Capacitively coupled Single Electron Tunneling (SC-SET) transistor.



Fig. 1. Superconducting loop with two SC-SET transistors. The circuit is symmetrically biased.

2. EXPERIMENT

Our circuit consists of two SC-SET transistors, connected in parallel to form a loop as shown in Fig. 1. We made samples using by four layers resists technique for making suspended bridges and shadow evaporation. This four layers resists system is composed of PMMA/Ge/photoresist/PMMA, where Ge layer is used as the window for shadow evaporation. After the exposure of top PMMA layer by electron-beam lithography, Ge was etched by CF4 in Reactive Ion Etching (RIE), and then etchant gas was changed to O2 for etching photoresist and PMMA to make under-cut under Ge layer. Bottom PMMA layer was used for easy lift-off. This technique gave us more precise size of junctions compared with the standard double layer resists (PMMA/co-polymer) technique. Each of the junctions were of size 0.01 μ m² and were made of Al/AlO_x/Al on an oxidized silicon substrate. The center electrode of each SC-SET was 1.0 µm long, and the mean area of the loop (1/2× (inner + outer area)) was $3.5 \,\mu m^2$.

Assuming a perfectly symmetric circuit, the normal state resistance of each junction is that of the entire circuit, $R_n=19.2k\Omega$. From this we can calculate a Josephson coupling energy, $E_J=34 \mu eV$. The capacitance of each junction is estimated from its size to become 0.5fF. Thus the sum of all capacitances to the central electrode becomes $C_{\Sigma}\approx 1$ fF or $E_C=e^2/2C_{\Sigma}=80\mu eV$ and $E_J/E_C=0.43$.

The capacitance of each gate to the central electrode was slightly different. We could compensate for this difference by attenuating one of the gate voltages by a factor α which could be adjusted by measuring the beating of each gate voltage modulation. In this way we could induce the same quasicharge on each gate capacitance by means of one voltage, $Q_{g1}=V_gC_{g1}$ = $Q_{g2}=\alpha V_gC_{g2}$, to better than 1% accuracy.





3. RESULTS

Figure 2 shows a three-dimensional (3D) plot of the I-V curves taken at various gate voltages for fixed magnetic field B=9.46 Gauss.

Here we see a periodic modulation of the *I-V* curve having period in gate voltage of e/C_g . We have not yet observed a $2e/C_g$ period in this type of circuit. We can identify the minimum of the current peak near zero bias voltage as the state where the quasicharge in the central electrode $Q_g=ne$ (n an integer). When $Q_g=ne$ or ne/2, the *I-V* curve is antisymmetric, I(V)=-I(-V). In addition, we can also see that the *I-V* curve is antisymmetric in Q_g , $I(V,Q_g)=-I(-V, -Q_g)$. The later antisymmetry, which is most visible at bias voltage $\pm 350\mu V$, is similar to the "Coulomb staircase," occurring in the C-SET configuration when the two tunnel barriers are not equal. For the current peaks below $250\mu V$ we see both gate voltage and magnetic field modulation.

Figure 3 shows a 3D plot of I-V curves in the low bias region, taken at various magnetic fields (*B*) for fixed gate voltage V_g =3.3mV. There is a periodic modulation in the magnetic field *B* having period 6.1 Gauss, which corresponds to within 6%, to one superconducting flux quantum Φ_0 =h/2e =20.7Gµm² in the mean area of the loop. This modulation in *B* is the strongest for the peak near zero bias voltage, and becomes progressively weaker at larger bias voltage.



Fig. 3. A 3D plot of *I*-V curves at the function of magnetic field B at the fixed gate voltage $V_g=3.3$ mV.

The modulation seen in Fig. 3 arises only if the Josephson phase is coherent when going around the loop. The theory of coherent Cooper pair tunneling (CCPT) has been discussed in the literature³), but previous experiments¹) have not verified phase coherence across both junctions in the SC-SET. It is not easy to identify features in the experimental *I-V* curve with the corresponding features in the theoretical curves³) due to the enormous amount of structure in both. Our data are in agreement with theory in that CCPT is dominant at low bias $eV < 2\Delta$, where we observe the largest modulation in *B*.

The interplay between gate voltage and magnetic field modulation in this low bias region is complex and cannot be described as a simple superposition. For example, we find that the largest amplitude of modulation in *B* occurs for the current peak near zero bias voltage, when $Q_g=ne$. This result seems counter intuitive as it means that CCPT is the greatest when the Coulomb blockade is maximum. Further analysis of this interplay will be the subject of a longer publication.

ACKNOWLEDGMENTS

This research was supported in part by the grant from the Japanese Ministry of Education, Science and Culture, and the Swedish NFR and TFR. One of author (Y.H.) acknowledges for the financial support from Scandinavia-Japan Sasakawa foundation. Our samples were fabricated in the Swedish National Nanometer Laboratory.

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