One-Dimensional Conduction of Ultra Fine Silicon Quantum Wires

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[Abstract] A novel fabrication method of the Silicon quantum wires has been proposed where anisotropic wet chemical etching and thermal oxidation are used to realize greater electron confinement by the physical structure. With this method, ultra fine Si quantum wires with nominal width of 65nm, which are fully contained within SiO2 have been successfully fabricated. Measurements of the electrical characteristics of such wires are also performed at low temperatures, and fine oscillations in Ids-Vgs curve are clearly observed. Assuming the origin of these oscillations is one-dimensional subband effect, the experimental results are in good agreement with the theoretical prediction.

1. INTRODUCTION

As the VLSI dimension approaches the nanometer scale, conventional Si devices will reach their operational limits. To overcome this problem, one of the possibilities is the low dimensional quantum devices. Toward that goal, the first step is to establish the fabrication method of the ultra fine structures of which dimension should be below 100nm. Recently Si quantum wires using metal-oxide-semiconductor (MOS) structures have been studied. Up to now, most Si quantum wires have been based on MOS structures where electron confinement is achieved by electrostatic confining potential via gate voltage (i.e. narrow gate over SiO2 [1], narrow mesas [2], or multiple narrow gates [3]). These approaches have some problems such as the channel wide uncertainty due to fringing fields beyond the gate [1,3], or degraded mobility due to scattering at sidewall ripples caused by dry-etching [2].

In this work, we attempt to establish one-dimensional confinement by physical boundaries, namely, Si quantum wires fully contained within SiO2 having both smooth Si/SiO2 interface boundaries and high potential barrier. The novel fabrication method of the above Si quantum wires using anisotropic wet etching and thermal-oxidation has been proposed. In addition, the electrical transport properties of the wires are examined to observe one-dimensional conduction.

2. EXPERIMENTAL

The sample fabrication process is shown in Fig.1. First, SiO2 mask patterns are fabricated on a n-type Si (100) substrate by the conventional lithography technique. Then, the Si substrate is etched down to a 250 nanometer depth to form shallow trenches. (Fig.1-(a)) Next, anisotropic wet chemical etching is performed with the EPW4 (E:ethylenediamine, P:pyrocatechol, W:water) etchant to form a saw tooth structure. Then, the Si nanostructure with a triangle cross-sectional profile is formed on top of the saw tooth. (Fig.1-(b)) After removing the SiO2 mask, the nanostructure is thermally oxidized so that the nanostructure is narrowed and electrically isolated from the substrate, simultaneously. As a result, ultra fine Si quantum wires, being fully contained within SiO2, are formed. (Fig.1-(c)) The n+ diffused source and drain electrodes are formed at both ends of the wires. Next, the CVD SiO2 is deposited and planarized. Then an aluminum gate electrode is formed above the CVD SiO2 to control the electron density. The final cross-sectional structure of the sample is shown in Fig.1-(d). In this sample, 100 parallel wires are formed to improve the signal-to-noise ratio[3]. The source and drain electrodes are electrically isolated from the substrate by the implanted p-type buried layer, which also eliminates the formation of the electron channels under the wires.

DC electrical measurements of the sample are performed at low temperatures. The excitation voltage Vsd between source and drain is kept small, i.e. ~200 µV, in order to avoid electron heating.

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3. RESULTS AND DISCUSSION

Figure 2 shows SEM image of the sample where SiO₂ layers and the Al gate electrode are removed for clarity. Ultra fine free-standing wires clearly show continuity of individual wires. Figure 3 is the cross sectional TEM image of the wire. The 65 nm wide wire has been successfully formed without any defects, and the Si/SiO₂ interface boundaries are very smooth. The width variation along the wire is within 5%. Using this new fabrication method, the ultra fine wires are prepared for observation of quantum effects.

Typical $I_{sd}$-$V_{g}$ curve (the wire current vs. gate voltage) at 4.2K is shown in Fig.4. The fine oscillations of the wire current are clearly observed. The oscillations in $I_{sd}$-$V_{g}$ curve persist up to $\sim$20K, and up to few meV of $V_{sd}$. The origin of these oscillations has been discussed in terms of universal conductance fluctuations (UCF) [5], or hopping[6].
These random phenomena can be averaged out, since our sample has 100 parallel and identical wires suitable for observing one-dimensional subband effect.

Therefore, as shown in Fig.5, the origin of the current oscillation can be explained by the one-dimensional nature of the electron system in the wire. In this case, the wire current should have localized peaks when the Fermi level \( E_f \) of the wire, being controlled by the gate voltage, coincides with the quantized subband energy levels \( E_i \) of the one-dimensional quantum wires.

To verify the above explanation, theoretical values of \( E_i \) and experimental values of \( E_f \) are compared. The results are shown in Fig.6. The subband levels \( E_i \) are simulated by solving the Schrödinger's equation in the triangular cross section of the wire\(^7\), neglecting the deformation of the potential in the wire due to the electric field induced by the gate for simplicity. The Fermi level \( E_f \) at each peak in Fig.4 can be extracted by 2D approximation as follows;

\[
E_f = \pi \hbar^2 C(V_g - V_t)/2m^*
\]

Here, \( C \), \( V_g \), and \( V_t \) are the capacitance between the gate electrode and the wire, the gate voltage at each wire current peaks, threshold voltage, and the effective electron mass, respectively. The capacitance \( C \) is calculated using a device simulator 'SMART-II' \(^8\), taking the fringing field of the gate electrode into account. In above estimations, the effective electron mass \( m^* \) is assumed to be 0.98\( m_0 \). In Fig.6, they extremely agree with each other, which confirms that the oscillations arise from one-dimensional subband effect.

4. CONCLUSION

The proposed method realizes ultra fine Si quantum wires, which are fully contained within SiO\(_2\). The electrical characteristic of the wires is confirmed to be of typical one-dimensional conduction. Further investigations using this fine wire will bring us more useful information about the low dimensional Si quantum effects.

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