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Si LSI as a Post Si LSI

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History of LSI Devices which improved early day's LSI performances is introduced. Recent and near future LSI technologies are reviewed. To overcome physical limitations of current VLSI technologies, an XMOS transistor is introduced for a sub-0.1 micrometer LSI device. Finally, the number of carriers in a low sub-0.1 micrometer channel is examined and found to be small enough to realize 'single electron' operation in low sub-0.1 micrometer future LSI devices.

1. Introduction

Continuously increasing processing steps and complexity in interconnection and architecture of VLSI's have been one of key issues to be solved for realizing cost effective VLSI chips. In spite of the above continuous discussion, number of photo-masks increased from 4 in late 1960's to around 25 for current RAM's and number of the interconnection also increased from a single Al layer with a diffused cross under to 4-6 metal layers for logic circuits, for incessant improvement in integration density and circuit performance.

Whenever limitation of Si LSI was discussed, some technology, e.g. the GaAs IC or Josephson Junction IC was referred to as a 'post silicon LSI' technology and R&D budget had been increased for these 'promising' technologies especially in universities and government laboratories. However, newly emerged processing technologies replaced the conventional ones to overcome the limitations, such as '1.25 micrometer discrepancy' and 'half micrometer barrier in optical lithography' [1]. Super resolution technologies [2] and excimer laser lithography [3] have made the half micrometer lithography barrier as a mirage. Silicon LSI's are still flourishing today.

2. Early day's technologies

Although basic MOS processing technologies such as sodium-less processing technologies and the (100) orientation silicon substrate were already being developed, many device/circuit technologies were developed to do with the early phase premature IC processing technologies. A bias stabilized analogue circuit for MOS transistors with drifting Vth [4], a Schottky diode clamp technology [5][6] to eliminate the gold diffusion which reduced chip yield in old digital bipolar IC's, and the DSA MOS transistor [7] to realize an effective sub-micrometer channel with high drain breakdown voltage by early phase (5 micrometer level) lithography are some first examples.

The n-channel MOS technology [8] and E/D MOS technology [9][10] as improved high speed technologies over the p-channel E/E technology under a given design rule and a channel injection type floating gate memory [11] as an n-channel compatible high speed/high integration technology over the p-channel FAMOS [12] are the second phase examples. The E/D MOS technology also was replaced by the CMOS technology [13], which had been invented earlier, to realize lower power dissipation with a penalty of additional processing steps.

The one-transistor-one-capacitor DRAM (1Tr DRAM) [14] as a high density memory technology over SRAM is one of the most important examples to be mentioned. With the silicon gate technology, LOCOS technology, ion implantation technology and dry etching technology, which were invented or introduced into the LSI process at a similar time, the 1Tr DRAM has been integrated as was proposed, as far as its circuit diagram is concerned. However, the structure and building materials of the capacitor became too complex to be of low cost and the conventional DRAM should be replaced by a new cell based on an innovative device/circuit concept e.g. a gain cell to reduce the complexity in the processing technology and to enhance compatibility with ASIC process.

2. Current and near future technologies

Fig. 1 shows a flow of LSI technologies with reference to LSI generations. For an MOS transistor in an LSI of 0.13 micrometer generation, thin gate oxide less than 5nm in the thickness and shallow source/drain junctions less than 50nm in

the depth will be used.

Optical lithography, ArF excimer laser lithography will be used to define device/circuit patterns.

Foradry etching technology, selectivity of etching rate of the gate materials to the thin gate oxide should be more than 100 and for reproducible gate length, CD loss of the dry etching is required less than 7nm with excellent anisotropy and negligible charging damage. The single wafer process for precise etching control also requires a high etching rate more than 300nm/min to maintain a high through-put. These requirements will be achieved by a lower pressure and higher density plasma, such as helicon wave plasma, ICP or improved ECR plasma in a high pumping rate chamber. Oxide etching for contact and via holes will be more complex with its gas chemistry to control composition of carbon rich polymers. However, experts have solutions to it.

The thinner the gate oxide becomes, the more contamination-less and atomic level surface preparation and defect free oxidation are required. The shallow source/drain will be realized by low kV acceleration ion implantation and an RTA process with improved defect control. Sheet resistance of the shallow source/drain of this generation may sometimes be too high even for consumer-use LSI's and a salicided source/drain becomes an important option.

Number of the interconnection layers on an LSI will amount to 6 and processing steps for the interconnection rules cost of the LSI. CVD barrier metals will be already used for high aspect ratio (~5) contacts and vias. Cu and low k inter-layer dielectrics will be of a high reliability option and of a high speed/low power option, respectively.

3. Beyond 0.13 micrometer feature size

There have been leading arguments on economy and design capability of an LSI beyond the 1Gbit generation. However, when we cease to develop new devices and processing technologies of an LSI, design people themselves cannot enjoy picking-up flowers and crops in the coming LSI field. I should like to return to seek future seeds in an LSI technologies rather than being trapped in the fruitless criticism.

One of the most critical processing technologies is lithography. Optical lithography has been and will be used for production of LSI's, as far as it is available. However, beyond 0.13 micrometer feature size, an optical system of lithography will be drastically changed from a current stepper lens system, if any. Although there exist strong light sources with shorter wave lengths than ArF excimer laser, no probable optical nor X-ray lithography system is yet seen. Electron beam lithography might be the alternative, however, its throughput should be and may be improved.

Fig.2 shows number of channel impurity atoms in the depletion layer of a unit channel of an MOS transistor with equal channel length and width. The number becomes 'countable' and deviation in Vth value due to a statistical distribution of channel impurity [15] becomes of a practical concern, because it will be one of main causes of circuit yield beyond the 0.13 micrometer feature size [16]. A novel uniform doping technology or an alternative transistor design concept will be necessary.

An XMOS transistor [17], a depleted channel of which is sandwiched by a lower gate and upper gate as shown in Fig.3, is one of candidates to realize sub-0.1 micrometer devices with improved punch-through immunity and Vth controllability without using any channel impurity. The device can be realized by one of SOI technologies. The device concept will be applicable down to channel length of 0.02 micrometer with channel thickness of 5nm as shown in Fig.4 [18].

Number of electrons (or holes) of a unit channel is also shown in Fig.2. Less than 10 electrons in the unit channel at sub-0.1 micrometer region suggest possibility of a big telegraph noise [19] which is generated by interface states capturing and releasing the channel carriers. Atomic level control of Si-SiO2 interface will become of further importance. However, the small number of electrons in a channel also suggests 'single electron' or 'countable electron' operation [20]. Devices different from having been widely discussed counterparts [21] and manufacturable by an extension of current VLSI technologies will be proposed in near future. The single electron operation will be an ultimate approach to realize a circuit dissipating the lowest power on an LSI chip at room temperature. [22]

4. Conclusion

Considering history of early day's LSI devices which improved the performance of LSI's not by improvement in the processing technology new device concepts again will be required to overcome physical limitations in current processing technologies and device design in a sub-0.1 micrometer region. An XMOS transistor was introduced to overcome the effect of statistical impurity distribution in the channel of a MOS transistor. Single electron or countable electron operation in low sub-0.1 micrometer devices with the lowest power dissipation was suggested.

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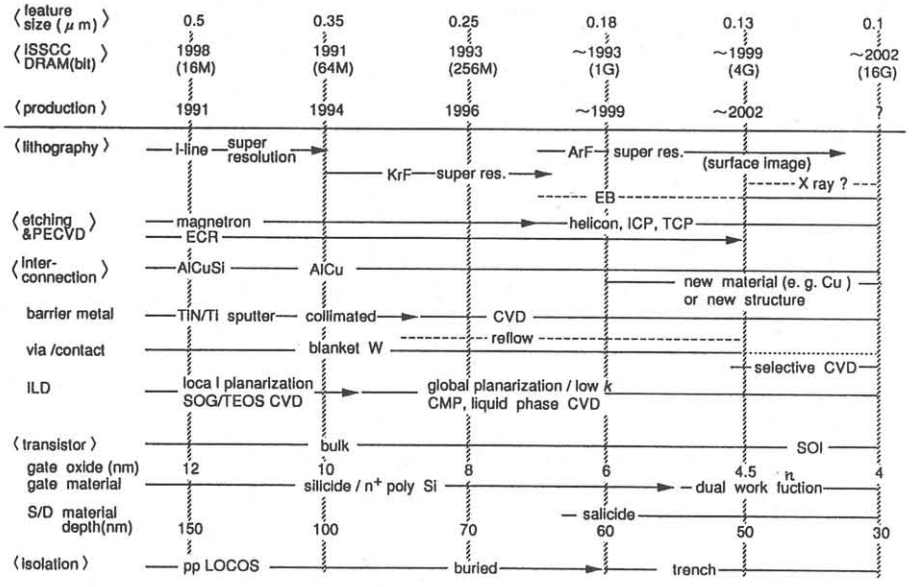

Fig. 1 Flow of VLSI technologies

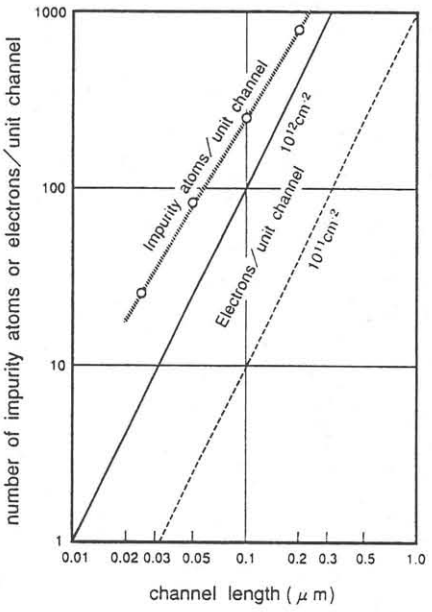

Fig. 2 Number of impurity atoms and electrons per unit channel.

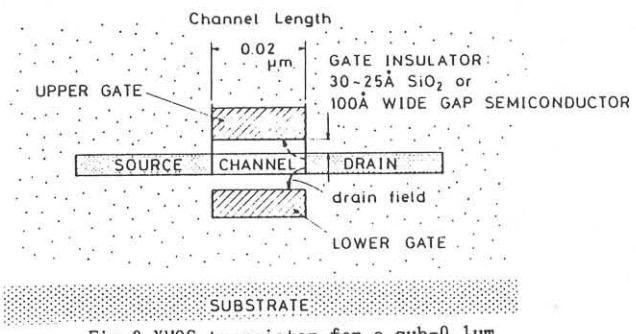

Fig. 3 XMOS transistor for a sub-0.1μm device without channel impurity.

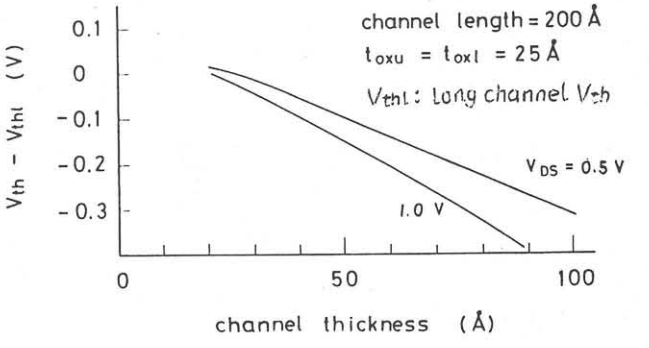

Fig. 4 (b) Channel thickness dependence of Vth of XMOS transistors.