

Invited

SOI Technology for VLSI

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Silicon-On-Insulator (SOI) technology promises improved performance and functionality in both digital and analog VLSI technology, in addition to that afforded by direct scaling. Performance enhancement results from the reduction of parasitic capacitances to the substrate and in a more subtle way from the presence of the floating body during the switching transient. In addition to performance improvement, SOI allows for a simpler process flow and perhaps even a smaller die size with concomitant improvements in yields. Thus the combined advantage of improved performance, lower integrated processing cost, and a potential transparency to bulk device and circuit design, make SOI a potential replacement for bulk Si substrates in an existing Silicon line. For this to happen however, significant progress in the development of a SOI materials' infrastructure is necessary. In this talk we examine the principal device considerations and progress towards the development of a materials' infrastructure especially for bonded SOI.

Introduction

Research on Silicon-on-insulator (SOI) has been steadily increasing over the last few years, and the advantages of fabricating CMOS circuits on SOI substrates is being seriously addressed by several development labs worldwide. The reader is referred to the excellent monograph on the subject by J.-P. Collinge¹ and references contained therein and also the proceedings of the IEEE SOI (or SOS/SOI) conferences², the ECS SOI conferences³ and Wafer Bonding Symposia⁴ as well as the SOI sessions in this meeting for a more extensive discussion. There have been several reports of dramatic performance improvements resulting from the use of SOI substrates⁵. SOI substrates have established themselves in the field of analog and mixed signal applications⁶ as well as certain smart power applications⁷. As SOI establishes itself in these specialized markets, its use is being investigated for mainstream digital CMOS applications both for logic and memory. The digital IC applications are projected to drive the SOI wafer market to over ¥ 20 billion over the next few years followed by further rapid growth.

Device Considerations

There are basically two structural options available for CMOS device implementation in SOI. In the first option (a) - called *fully depleted* - the thickness of the SOI layer is less than the depletion width in the channel region of the device. Such a structure, has several features: a nearly ideal sub threshold inverse slope of ~60mV/decade; a reduction of all parasitic capacitances to the substrate by about 25% or more; reduced short channel effects due to the film

thickness defined shallow junction depth. Other advantages are a potential increase in channel mobility (because of a smaller vertical surface field), and increased transconductance (because of a reduction in C_D - the depletion capacitance and also increased mobility). As a result the fully depleted FET has a higher drive capability. Fully depleted devices do not exhibit the so-called "kink" effect. Fully depleted devices may be operated either in the inversion mode or the accumulation mode with convenient V_t for CMOS obtainable with a single gate material⁸. The biggest disadvantage of the fully depleted devices is a stringent requirement on the thickness of the SOI layer and its uniformity. The threshold voltage for a given channel doping is extremely sensitive to the SOI film thickness. This is perhaps the biggest drawback of fully depleted devices, though a constant channel implant dose will reduce this sensitivity. The extremely thin SOI layers will need more sophisticated processing capability.

Non-fully depleted (sometimes called *partially depleted*) structures resemble more conventional scaled MOS transistors. they do not exhibit the extreme sensitivity of the threshold voltage to SOI thickness. They are more 'bulk-like' in that there is a neutral body. Unlike the bulk case this body is floating, (though it may be tied through the use of a special body contact). The depletion capacitance C_D is reduced, but not as much as in the fully depleted case. To first approximation, at least structurally, the technology is a bulk technology but on an SOI substrate. However, the operation of the partially depleted SOI MOSFET is some what more subtle⁹. The parasitic lateral bipolar transistor and its floating base i.e., the so-called floating body, play a complex

role leading to an anomalous increase in inverse sub threshold slope at high V_{DD} . The net effect is an effective increase in drive capability. It appears that for a given process and design technology these effects can be well controlled¹⁰. A concern is snapback or the inability to turn the device off, if the drain voltage is too high. This breakdown of the transistor can be avoided (as in the bulk case) by ensuring a low enough operating voltage. Tying the body to a fixed potential has been suggested, but will reduce the device packing density (by as much as 30-40%) and may also detract from the beneficial effects of the floating body. One possible concern is the possibility of some as yet unknown circuit sensitivity to the floating body potential fluctuations. A related effect is the "kink" in the output characteristics. P-channel transistors do not show the kink except at very high voltages. While the appearance of this kink is unacceptable for devices where linearity is a key (analog applications) it is quite tolerable (and even advantageous) for digital applications.

Another general point that must be made concerns reliability and operating voltage. It is clear that effects such as snapback and other reliability concerns are minimized at lower operating voltages. Bulk CMOS is also being driven to lower operating voltages by both reliability and market requirements for lower power operation. The performance improvement provided by CMOS/SOI can be traded for lower power operation, and this is clearly an additional driving force for SOI.

As a result of the foregoing SOI/CMOS offers some immediate advantages from a performance standpoint. It offers a way of effectively lowering the threshold - a normally non-scalable property (unless one lowers operating temperatures). The higher drive current speeds up the switching transient and manifests itself in improved performance. Additionally it is possible to lower the operating voltage and operate at a reasonably high performance level with respect to bulk. This approach to attain low power circuits is receiving widespread attention and will be an effective technology driver. The reduction of parasitics is also an important factor and alone may be able to contribute as much as 30% in performance improvement. Other advantages of SOI circuits is their increased radiation immunity and the possibility of easy integration of bipolar circuits for BiCMOS applications. This last application does require excellent lifetime in the SOI material. Low junction leakage (mainly because of reduced junction area) is another advantage of thin SOI that can be exploited in high temperature applications.

Besides performance, cost is another driving force for the implementation of SOI. There have been detailed studies¹¹ on the process simplification that a migration to SOI will bring about. Mainly, these stem from the simplification in isolation schemes. The elimination of the well implants and the ability to butt certain devices not only reduce processing complexity, but can significantly reduce die size and an increase in overall yield.

However, the biggest cost benefit derives from economic reasons. The performance improvement in SOI is available without further scaling. Traditionally, in CMOS technology, performance improvement has derived from scaling. This is increasingly a more expensive exercise and over time has necessitated the development of larger wafer diameters, more robust and uniform processes, and new tools. Today it is estimated that a new state of the art facility may cost upwards of ¥100 billion. The ability to extend the life of this facility by changing the substrate from bulk Si to SOI is an attractive proposition. If the facility depreciation has already been amortized over the life cycle of a previous bulk product, only the operating costs for the SOI product are relevant. These, as we have discussed promise to be lower for an SOI product, with the possible exception of the SOI substrate itself. The point to be made is that notwithstanding the higher price of an SOI substrate, migrating CMOS technology to SOI, especially if one is able to utilize a partially depleted design, where bulk designs can be ported to SOI with minimal changes, will provide a lower overall cost for the product. Additionally, SOI may offer the most viable path today, for the migration to lower power CMOS. Many of these points have been exemplified in recent work by Shahidi et al¹², where a 512K SRAM with about 1.5X performance improvement over bulk was achieved using bulk like technology on SOI. Furthermore the relative performance improvement over bulk increased at lower voltages.

There have been a few suggestions of novel memory structures utilizing SOI substrates¹³. Often, these are quasi three-dimensional structures where the storage node is fabricated on one level and the addressing device is on another level. Once again, junction areas are minimized so that leakage currents are less. SOI for memory applications will more likely require thicker device layers over 1µm. It is possible that such novel memory structures may provide our only approach DRAM structures at the 1Gbit level. The use of SOI in SRAMs has been quite widespread¹⁴ especially for radiation hard applications¹⁵.

Materials Considerations

Si technology owes its pre-eminent position entirely to the ready and cost effective availability of the bulk polished Si substrate. Similarly, the success of SOI technology is dependent on the availability of a similar quality SOI substrate. For the thickness range being considered for digital CMOS applications, there are two main SOI materials approaches that merit serious consideration: These are SIMOX (separation by implantation of Oxygen)¹⁶ and the bonded wafer approach¹⁷. The bonded wafer approach offers almost unlimited flexibility in that the thickness of the silicon device layer and the buried oxide (BOX) as well as the electrical characteristics of the SOI layer and the substrate, can be independently chosen. Throughout, it has been the material of choice and bonded SOI is extensively used in various analog and mixed signal products with great success. The main reason for this widespread acceptance is the excellent quality of both the superficial silicon and the buried oxide - unmatched by any other technique - and its availability at reasonable cost. Several surveys, including one conducted by the Japanese Electronic Industry Development Association (JEIDA)¹⁸ have indicated the preferability of the bonded wafer approach to SOI over other approaches by both merchant semiconductor houses as well as wafer manufacturers.

While Simox has been used extensively in the demonstration of many of the advantages of thin film SOI, the use of Bonded SOI has lagged. The biggest drawback of the bonded wafer approach has been the *perception* that it would be impossible to extend into the thin Si thickness regime of CMOS viz. 100-200 nm, with uniformities better than a few percent. However, over the last two years, important developments in bonded wafer fabrication have made the availability of *thin and uniform* bonded SOI at competitive price a reality. One approach is the Acuthin™¹⁹ method. Here a conventional bonded pair that has been thinned by grinding and polishing to below about 10 μm with ttv 's of a few μm is accurately mapped and locally polished using a plasma process. The wafer is scanned under the plasma head, and the dwell time dictated by the initial thickness and the target thickness. This method, combined with an efficient metrology system allows for the production of high quality thin SOI. Such wafers are available commercially.

The bonded wafer approach to SOI using an etch stop called Bond and Etchback SOI (BESOI) was proposed by Lasky et al²⁰. In their approach, an undoped epitaxial film is grown on top of a highly p^{++}

doped substrate. This layer is joined to an oxidized handle wafer (or oxidized and joined to a handle wafer). The p^{++} layer is then selectively etched off to stop at the i-layer. This original approach worked in principle but had some practical limitations. Since then there have been several new enabling technologies such as advanced epitaxial technology and sophisticated double etchstop technology that allow for a far more robust and uniform process²¹. The reader is referred to an excellent review by Maszara for a description²². BESOI wafers are also available commercially.

Today, surface morphology of all types of SOI wafers are inferior to that available in bulk Si wafers, though at long wavelengths, SOI surfaces are comparable. At shorter wavelengths, the BESOI roughness is very sensitive to the final etch or polish step employed, and can be made comparable to bulk Si after sacrificial oxidation. The epitaxial BESOI film also important to obtain good gate dielectric quality and reliability and its good crystallinity and purity is evident from lifetime measurements. Effective lifetimes as high as 370 μsec , comparable to bulk have been obtained on BESOI. This is indicative of excellent quality of *both* the SOI film and the oxide interfaces. Film uniformity - a key concern for bonded wafers - of better than $\pm 3.5\%$ at thicknesses as low as 100nm are routinely obtainable by BESOI on all diameter wafers with an edge exclusion of $<6\text{mm}$. The ability to "dial-in" SOI and BOX thickness has also been amply demonstrated in BESOI.

Sheet resistance and spreading resistance measurements indicate that the carrier concentration is well below 10^{15} cm^{-3} . Carbon and oxygen concentrations are also below detectability limits. Transmission Electron Micrographs fail to show dislocations or any delineation of the bonded interface. No Si inclusions - a common occurrence in Simox are observed. Independent measurements of the buried oxide integrity and charge show it to be similar to thermally grown oxides. The BESOI films synthesized by the methods detailed above have been used in the fabrication of CMOS devices and circuits. The details of the process and the results are described elsewhere²³. Delays as low as 20 psec have been reported for channel lengths of about 0.1 μm at 1.7V. Sub 50 psec delays at 1 V bias for bulk and BESOI devices are also very impressive. These results clearly demonstrate the applicability of BESOI to high performance and low power CMOS technology, and coupled with the potential to lower costs of CMOS by SOI fabrication processes and the inherent quality of an epi-based SOI materials technology promise widespread use of BESOI for

digital applications in the sub100nm to 2.5 μ m range. The ability to reduce the operating power supply and yet exhibit very high performance bodes well for the use of SOI for low power and portable applications.

Conclusions

In summary, a convincing argument for the application of SOI to CMOS can be made from both cost, performance, and low power considerations as well as additional functionality. We expect the insertion of SOI at the 0.5 to 0.25 μ m lithography generation using partially depleted designs. The ready availability of cost effective substrates on a manufacturing scale is

crucial before semiconductor manufacturers can commit to SOI based product programs. Simox and Bonded SOI are the main options. The bonded wafer approach, especially BESOI, offers the potential of cost effective, high quality epitaxial film SOI substrates on a manufacturable scale. It is the only current SOI technology that uses readily available commercial semiconductor processing equipment, and shows reduced per cm² cost as the wafer diameter is scaled up. The entry of mainstream silicon suppliers into the SOI business and a sustained push by chip makers into manufacturing, promise to make SOI a reality.

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