Invited

High Performance 0.1 μm CMOS Devices

K.F. Lee and R.H. Yan*

AT&T Bell Laboratories

Murray Hill, NJ 07974; *Holmdel, NJ 07733

Abstract

Design issues for 0.1 μm devices, in particular the role of junction depth in short channel effects, are discussed. A high performance room temperature CMOS technology with gate feature size in the 0.1 μm regime is described. The design seeks to demonstrate the performance capability of the intrinsic device. Unloaded ring oscillator gate delay of 11.8 psec at 2.5 V, and 14.4 psec at 1.5 V, has been demonstrated.

Introduction

If the current pace of device miniaturization continues unabated, 0.1 μm devices will be in production some time in the next decade. Many technological challenges to fulfilling this remain. In this work, we focus on the important parameters in intrinsic device design and optimize performance by the reduction of parasitics.

Device Design and Junction Depth

According to conventional scaling[1], suppression of short channel effects requires gate oxide thickness to be reduced, the substrate doping to be increased, and the junction depth to be reduced. Recently, it has been shown that these requirements are overly restrictive. Yan et al[2] described a "vertical-doping-engineered" structure with a heavily doped region below a lightly doped channel region. The heavily doped region acts as a ground plane, imposing a boundary condition on the solution of Poisson equation in the region above the ground plane. Drain induced barrier lowering DIBL for a given channel length is determined by t_{ox}, the oxide thickness, and t_{si}, the thickness of the lightly doped region above the ground plane. Other retrograde doping structures have been previously described[3,4,5]. Yan's analysis puts the design on a physical basis, and identifies parameters that are useful in guiding device design. Using such a structure, devices of good subthreshold control have been fabricated, and cut-off frequency of 116 GHz has been demonstrated in n-channel MOSFETs[6], and 51 GHz in p-channel MOSFETs[7].

Another property of the ground plane structure is that junction depth is not a parameter in affecting DIBL. Such a result has been exploited in the design of pMOS[7]. Such insensitivity to junction depth has also been shown by simulation in devices with retrograde doping[4].

The insensitivity to junction depth is not limited to vertical-doping-engineered devices. A uniformly doped substrate can be viewed as an extension of the doping in the ground plane region everywhere, in particular into the channel region. Devices with uniform substrate doping at sufficiently high concentration should have no worse DIBL than a retrograde doped device. Fig. 1 is a simulation of subthreshold slope vs junction depth for a uniform substrate doping of $1 \times 10^{18}/cm^3$. For devices at a constant channel length of 0.1 μm, it is seen that the subthreshold slope S remains constant. The effect of increased lateral diffusion due to junction depth needs to be considered. If a constant gate length is used, then as the junction depth is increased, lateral diffusion results in a shortening of the channel length. The resultant increase in S is due to channel length reduction, not from junction depth increase.
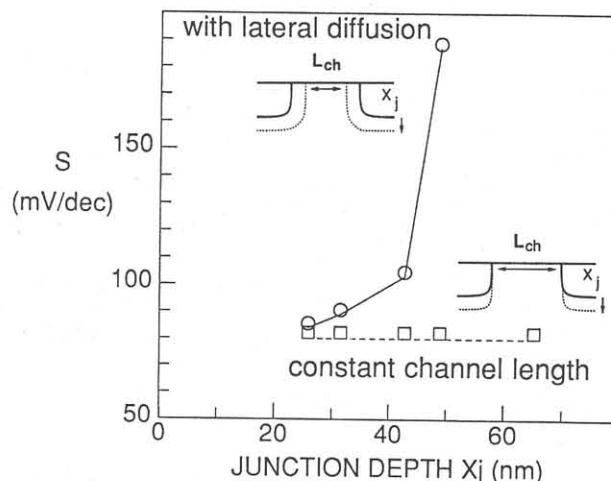

Fig. 1 Subthreshold slope vs junction depth $N_s = 1 \times 10^{18}/cm^3$, $t_{ox} = 4$ nm, $L_g = 0.1$ μm

Process outline

A cross-section of the CMOS devices is shown in Fig. 2[8]. Feature sizes obey g-line lithography design rules, except at the gate level. High intrinsic device performance is provided through a vertical-doping-engineered structure. Ways to reduce parasitic delay components due to junction capacitance, gate overlap capacitance and gate resistance are summarized as follows:

1. The channel implants are laterally confined by means of extra masking steps. This reduces the junction capacitance.
2. Device isolation and latchup resistance is provided by deep retrograde wells formed by high energy implant. The retrograde wells also keep the junction capacitance low.
3. Two-step sidewall to reduce gate-drain overlap capacitance in the pMOS device.
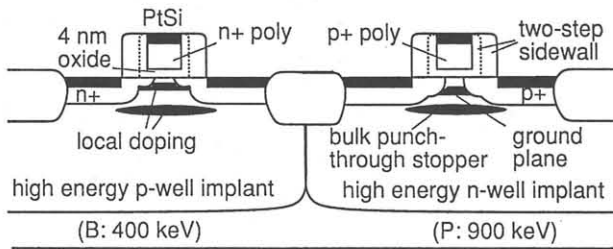4. Platinum salicidation to control gate sheet resistance at small dimensions.

Fig. 2 Cross-section of CMOS devices

The channel implant is a composite of two implants: a shallow implant with high peak doping to form the ground plane, and a deeper, moderately doped implant to prevent bulk punchthrough. The latter implant makes the device tolerant towards bulk punchthrough, which may occur below the ground plane if the junction depth is too deep. Fig. 3 is a simulated doping profile of the pMOS in the channel region. The kink in doping at around 0.2 μm is due to the bulk punchthrough suppression implant (Phos, $4 \times 10^{12}/cm^2$). The simulated subthreshold behavior

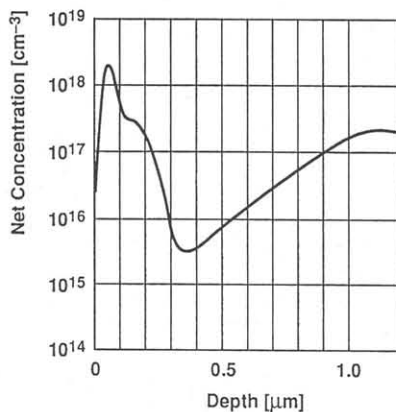Fig. 3 Simulated doping profile of the pMOS in the channel region

without the implant at $x_j = 0.12$ μm is shown in Fig. 4. A leakage current independent of gate bias exists at Vd=-2V, which increases with junction depth.
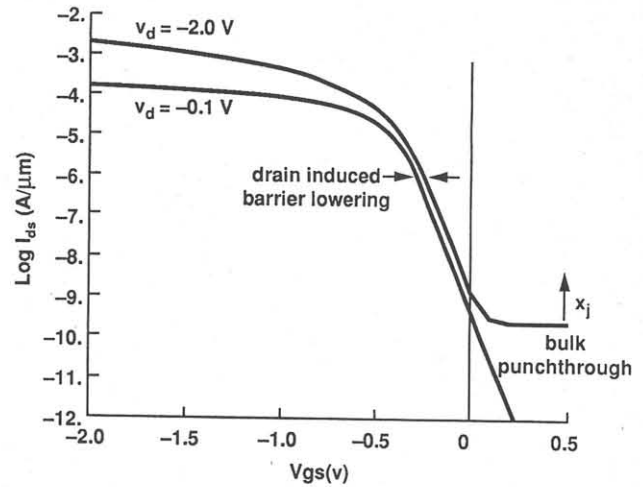

Fig. 4 Simulated subthreshold behavior of 0.1 μm pMOS device without a bulk punchthrough suppression implant, $x_j = 0.12$ μm

Experimental results

Fig. 5 shows the subthreshold slopes and threshold voltages of nMOS and pMOS devices as a function of gate length, measured at room temperature[8]. Fig. 6 shows the subthreshold behavior at 0.13 μm gate length. The drain characteristics of the same devices are shown in Fig. 7. Transconductances of 400 mS/mm and 300 mS/mm were obtained for the 0.13 μm gate length nMOS and pMOS device, respectively. Fig. 8 shows the gate platinum silicide sheet resistance as a function of gate length. A sheet resistance of about 5 Ω/□ was maintained. The junction leakage in both the n^+ and p^+ junctions is on the order of 100 nA/cm^2. Since this design is tolerant towards deep junctions, the junction leakage can be further optimized.
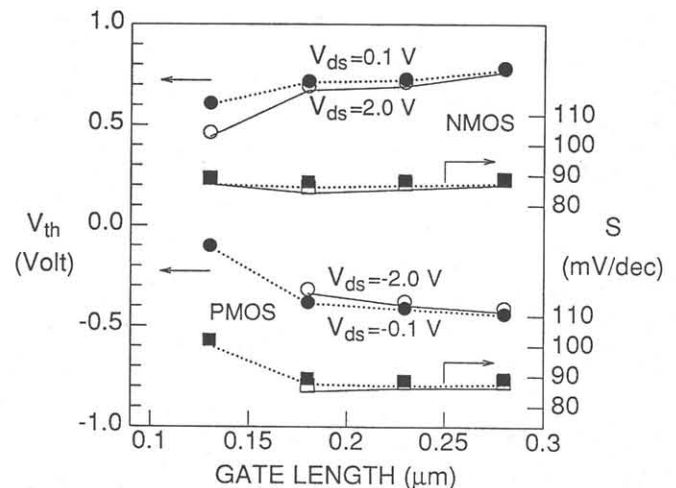

Fig. 5 Subthreshold slopes and threshold voltages (1 μA) of nMOS and pMOS as a function of gate length, W=9.5 μm

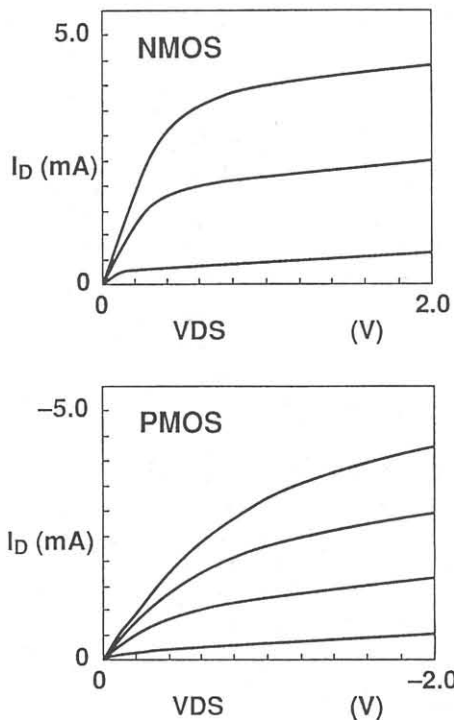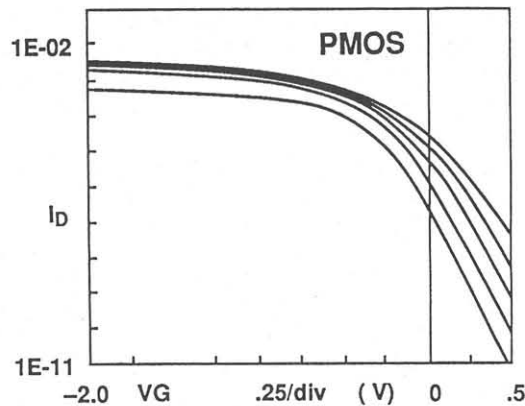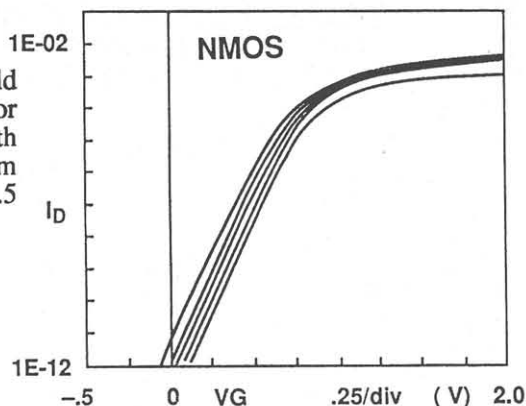Fig. 6 Subthreshold characteristics for 0.13 µm gate length devices. $|V_{ds}|$ from 0.1 V to 2.0 V, W=9.5 µm

NMOS
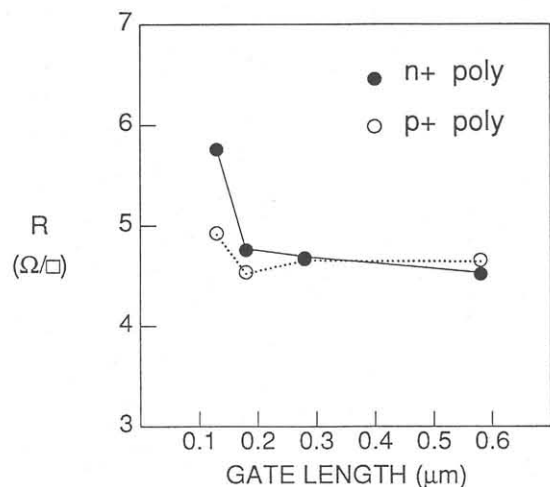
PMOS

Fig. 7 Drain characteristics. $|V_{gs}|$ from 0 V to 2.0 V

Fig. 8 Line width dependence of platinum silicide

Conventional, single-finger, unloaded CMOS ring oscillators ($W_n=W_p= 5$ µm) were fabricated. Gate delay as a function of gate length and power supply voltage is plotted in Figure 9[8]. At 0.13 µm gate length, delays of 11.8, 12.7, and 14.4 psec were obtained at 2.5, 2.0, and 1.5 V, respectively. The delay of 11.8 ps is a record for a CMOS technology. Various analog and digital circuits have also been fabricated. These include a frequency divider operating at 13.4 GHz[10], and a phase-locked loop at 3 GHz[11].
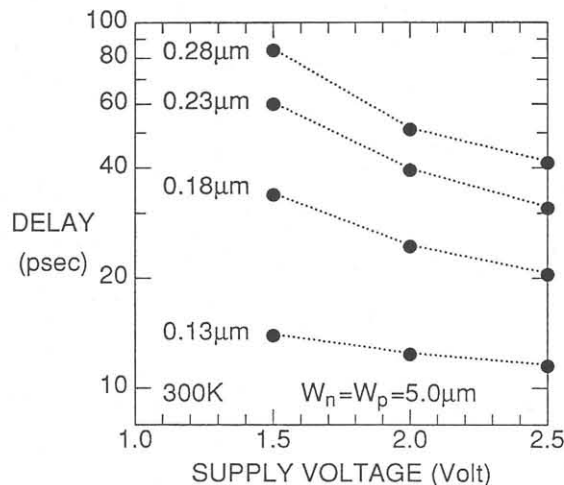
Fig. 9 Unloaded gate delay as a function of power supply voltage and gate length

Conclusion

We have demonstrated the capabilities of a 0.1 µm bulk CMOS technology. A record gate delay of 11.8 psec at 2.5 V has been obtained.

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