Hot Carrier Effects in Sub-0.1 μm MOSFETs


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The behaviors of the substrate current and impact ionization rate are thoroughly investigated in a wide temperature range for ultra-short channel MOSFETs. New important features are shown for the variations of the maximum substrate current as a function of applied biases and temperature. It is also shown that the conventional $I_p/I_Q$ plots do not give a single straight line for a given technology in the case of deep submicron devices, and are function of channel length and applied gate and drain biases. Furthermore, it is demonstrated that this kind of plots is not reliable for the comparison of hot carrier effects in the case of sub-0.1μm transistors. A direct comparison of the impact ionization rate for constant drain voltages and $(V_g-V_t)$ values is more meaningful. With this method, it is shown that, although a significant enhancement of hot carrier effects is observed by scaling down the devices, a strong reduction of the impact ionization rate is obtained for sub-0.1μm MOSFETs operated at liquid nitrogen temperature in the low drain voltage range.

1. INTRODUCTION

The substrate current is a powerful parameter in order to predict hot-carrier-induced degradation and lifetime in MOSFETs [1]. The impact ionization rate (M= $I_p/I_Q$), which suppresses the influence of the drain current $I_d$, is generally used for the comparison of hot carrier effects as a function of channel length or temperature. A very convenient method for the characterization of hot electron phenomena in MOS devices is the use of the plot $\ln(M)$ versus $1/(V_d-V_{dsat})$. The variable $(V_d-V_{dsat})$, which depends on the drain saturation voltage $V_{dsat}$, is very useful in order to obtain a single straight line for different channel lengths and gate voltages for a given technology [2]. However, deviations from this single line have been found in ultra-short channel MOSFETs, with some increase or reduction of the impact ionization rate with decreasing the gate length [3-5]. Moreover, recently, deviations from this single line have also been observed as a function of applied biases for very short channel MOSFETs [5]. Furthermore, recent studies have shown that hot carrier effects are always very harmful for deep submicron devices operating at low drain bias [4-5], even for $V_d=1.5V$ for MOS device in the 0.1μm range [5]. On the other hand, low temperature operation was supposed to enhance hot carrier phenomena, but recent studies have shown that the multiplication factor can be decreased as the temperature is reduced in the low drain voltage range [6-8]. The aim of this paper is to analyse thoroughly the variations of the substrate current and the impact ionization rate in a wide temperature range for sub-0.1μm MOSFETs. New important behaviors for the dependences of the substrate current and multiplication factor on applied biases and temperature are highlighted and qualitatively explained.

2. RESULTS AND DISCUSSION

In Fig. 1 are shown the variations of the substrate current with gate voltage as a function of $V_d$ for 300 K and 77 K in the case of a 0.07 μm gate length MOS device. As exemplified in Fig. 1a for 300K, the substrate current peak is obtained for a $V_g$ value ($V_{gmax}$) which is almost independent of drain voltage, unlike for long channel MOSFETs for which a strong decrease of $V_{gmax}$ is obtained with reducing $V_d$. On the other hand, at 77 K (Fig. 1b), $V_{gmax}$ substantially increases when $V_d$ is reduced, highlighting a very original behavior for these deep submicron MOS transistors. These features can be understood in figure 2 which presents the variations of the impact ionization rate $M$ ($=I_p/I_Q$) with $V_g$. For the 0.07 μm device of Fig. 1, it is clear that $M$ shows the most gentle slope with $V_g$ for low $V_d$ and at low temperature (Fig. 2a). This low reduction of the impact ionization rate with increasing the gate bias leads to an enhancement of the substrate current until high $V_g$ and induces a substantial shift of the substrate current peak. The comparison of the $M(V_g)$ characteristics as a function of channel length (Fig. 2b) shows that, at very low temperature, the slope of the curve for a very short transistor (0.07 μm) is substantially lower than that of a long transistor (0.5 μm). At room temperature, a smaller slope is also obtained in the case of the sub-0.1 μm MOSFET compared with the 0.5 μm transistor, which leads to a quasi-constant $V_{gmax}$ with $V_d$ for ultra-short channel devices in this temperature range. These behaviors will be very important for the aging conditions of sub-0.1 μm devices, and a degradation for $V_g=V_d/2$ will not lead to the maximum substrate current conditions.

On the other hand, it should be mentioned that a hump is observed in the $M(V_g)$ characteristics at low gate voltages for the 0.07 μm device (Fig. 2b). This hump is due to the accumulation of the LDD regions when $V_g$ is increased due to the gate fringing field effects associated with the polysilicon spacers. In fact, the influence of the source-drain series resistance $R_{sd}$ is very high for sub-0.1 μm MOS transistors, even at 300K with no impurity freeze-out in the LDDs, and $R_{sd}$ is substantially reduced when the LDD regions are accumulated. This effect induces an increase of the effective drain voltage and, therefore, an enhancement of the impact ionization rate. This behavior leads also to a substantial hump in the transfer $I_g(V_g)$ characteristics with a strong increase of the drain current for sufficiently large gate biases (Fig. 3). It should also be noted that this effect cannot be seen for the 0.07 μm device of Fig. 2a due to important short channel effects in this case, associated with a smaller effective channel length. A higher
drain leakage current is thus obtained, which prevents to observe this phenomenon at low gate voltage. Nevertheless, this device is also very useful in order to measure the substrate current at low temperature for relatively high drain voltages due to a significant reduction of the kink effect [9].

In figure 4a are plotted the variations of the impact ionization rate M as a function of 1/(V_d-V_dsat) for various gate lengths. The determination of V_dsat has been carried out with the conventional method of reference [2] which uses the plots of constant M values as a function of the gate and drain voltages. When the devices are scaled down, an increase of M, together with a reduction of the slope of the M(1/(V_d-V_dsat)) characteristics, are underlined in these figures. Figure 4b shows the dependence of M on 1/(V_d-V_dsat) for a 0.07 μm gate length MOSFET and various V_dsat values. A significant reduction of the slope of the characteristics is obtained with increasing the saturation voltage. On the other hand, a substantial deviation from the straight line is highlighted for large 1/(V_d-V_dsat) values. In order to understand this behavior, we have plotted in Fig. 5 the variations of the impact ionization rate versus V_d for various gate biases. A significant change in the slope of these curves is underlined for different gate voltages. It should be mentioned that the conventional model leads to parallel characteristics for different gate voltages [1,2]. Therefore, it is clear that this model cannot be applied for these ultra-short channel MOSFETs. These characteristics are in fact fully correlated with the previous one. A lower slope is obtained with increasing the gate voltage for both the M(V_d) and the M(1/(V_d - V_dsat)) characteristics. Besides, the determination of V_dsat with the conventional model of [2] generally used in the literature, cannot be applied for these deep submicron devices. In fact, the saturation voltages determined with this method will depend on the M values which have been chosen for the extraction. For instance, in the case of the 0.07 μm device shown in Fig. 5, a shift of about 0.1 V can be obtained depending on the impact ionization rate magnitude used for the determination of V_dsat. This shift will be highly important for the M(1/(V_d-V_dsat)) plots, and can lead to a significant enhancement or reduction of the impact ionization rate for very short channel MOSFETs, and, thus, M can be decreased or increased for 0.1 or sub-0.1 μm transistors compared with long channel ones. This behavior can in part explain the conflicting results which have been presented previously for ultra-short channel devices [3-5]. Therefore, these kinds of M(1/(V_d-V_dsat)) plots cannot be used in order to compare hot carrier effects for MOSFETs in the deep submicron range. A direct comparison of the impact ionization rate for constant drain voltages in the maximum substrate current condition, or, with a better method because of the original variations of the substrate current peak, for given (V_g - V_t) values, is therefore more meaningful. The variations of the impact ionization rate with V_d in a large temperature range in the maximum substrate current condition (M_max) and for a given (V_g - V_t) bias (M) are shown in Fig. 6. M_max increases slightly for V_d=1.8V when the devices are scaled down, and shows a minimum as a function of the gate length for V_d=1.5V, in particular at low temperature, with a similar multiplication rate in the 0.5μm and in the sub-0.1μm ranges (Figs. 6a-b). Therefore, it seems that hot carrier effects will not be so harmful for ultra-short channel MOSFETs. However, a very different behavior is obtained for the variation of M measured for a given (V_g - V_t) value (Figs. 6c-d). A substantial enhancement of M is found when the devices are scaled down for both V_d values, with a significant reduction for liquid nitrogen temperature operation. The best low temperature improvement at 77K for low drain bias (1.5V) is observed for the shortest (0.07μm) MOSFET. These differences between the M and M_max variations are due to the original shift of the maximum substrate current peak for low drain voltages in the case of sub-0.1μm devices (Fig. 1).

The M(V_g), M(V_d) and M(1/(V_d-V_dsat)) behaviors are explained in terms of pinch-off length and carrier mean free path variations. In fact, in our devices, the theoretical pinch-off length (70 nm) given by the conventional relation [1] is larger than the effective channel length for the 70 nm gate length MOSFET (in the sub-50 nm range). Therefore, this feature induces a substantial enhancement of the maximum lateral electric field. A second phenomenon is associated with the extension of the channel farther from the interface with scaling down the devices. This can lead to a significant enhancement of the carrier mean free path which induces an increase of the multiplication factor. Both effects can be responsible for the reduction of the slopes of the previous characteristics versus V_g, V_d and 1/(V_d-V_dsat). Furthermore, both effects will also lead to a substantial enhancement of the impact ionization rate for ultra-short channel transistors, which is observed in the case of a meaningful comparison (Figs. 6c-d). The extension of the channel far from the interface can also induce a lower average V_dsat value for a given (V_g - V_t), which also gives an increase of M in the deep submicron range. On the other hand, non-stationary effects are significant in our devices due to the small pinch-off length, even for long channel MOSFETs, associated with the small gate oxide thickness and junction depth, and become larger when the temperature is reduced. For the shortest devices (sub-0.1 μm) and the lowest drain bias (1.5V), the small pinch-off length (limited by the effective channel length) together with the sufficiently low electric field (at low V_d) induce a strong reduction in the number of high energy electrons at low temperature. Therefore, for V_g=1.5V, although the electric field is higher for sub-0.1 μm devices compared with longer transistors, the best liquid nitrogen temperature improvement for the impact ionization rate is observed for the shortest MOSFETs (Fig. 6d).

3. CONCLUSION

The behaviors of the substrate current and impact ionization rate have been thoroughly investigated in a wide temperature range for ultra-short channel MOSFETs. New important features have been shown for the variations of the maximum substrate current as a function of applied biases and temperature. It has also been shown that the conventional I_p(V_g(1/(V_d-V_dsat))) plots do not give a single straight line for a given technology in the case of deep submicron devices, and are function of channel length and applied gate and drain biases. Furthermore, it has been demonstrated that this kind of plots is not reliable for the comparison of hot carrier effects in the case of sub-0.1μm transistors. A direct comparison of the impact ionization rate for constant V_d and (V_g - V_t) values is more meaningful. With this method, it has been shown that, although a significant enhancement of hot carrier effects is observed by scaling down the devices, a strong reduction of the impact ionization rate is obtained for sub-0.1μm MOSFETs operated at liquid nitrogen temperature in the low drain voltage range.

Fig. 1: $I_P(V_g)$ characteristics for a 0.07 $\mu$m gate length MOSFET's for (a) 300K, and (b) 77K.

Fig. 2: Impact ionization rate $M$ versus gate voltage for (a) a 0.07 $\mu$m gate length MOSFET's for various temperatures and drain bias, and (b) 0.07 $\mu$m and 0.5 $\mu$m gate length MOS transistors for low drain voltage (1.5 V) and various temperatures.

Fig. 3: $I_d(V_g)$ transfer characteristics for a 0.07 $\mu$m MOSFET's in linear operation ($V_d=50mV$) as a function of temperature.

Fig. 4: Variations of $M$ as a function of $1/(V_d-V_{dsat})$ (a) for various gate lengths ($V_{dsat}=0.3V$ for all the devices), and (b) for various saturation voltages in the case of a 0.07 $\mu$m gate length MOSFET.

Fig. 5: Variations of $M$ as a function $V_d$ for various $V_g$ for a 0.07$\mu$m gate length MOSFET. A negative $V_d$ shift of 0.4 V has been used for the curve with $V_g=2.5$ V.

Fig. 6: (a-b) Variations of the impact ionization rate in the maximum substrate current condition ($M_{max}=I_{pmax}/I_d$) versus $L_g$ at 300, 200 and 77 K; (a) $V_d=1.8V$ and (b) $V_d=1.5V$. (c-d) Impact ionization rate ($M=I_p/I_d$) as a function of $L_g$ for a constant ($V_g-V_t=1.2V$) value at 300, 200 and 77 K; (c) $V_d=1.8V$ and (d) $V_d=1.5V$. 

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