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Kink Effect in 0.1 μm Bulk Si MOSFETs

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The kink effect is thoroughly investigated in a wide temperature range for 0.1μm and sub-0.1μm single-drain and LDD MOS devices. It is found that the kink effect can be observed even at room temperature for sub-0.1μm bulk Si MOSFETs. On the other hand, it is shown that short channel effects, observed in the deep submicron range, lead to reduced kink effects and allow to measure the substrate current for high drain biases and low temperatures, due to a lower variation with V_d of the barrier height at the source/substrate junction.

1. INTRODUCTION

The kink effect is very well known for SOI MOSFETs. It is one of the main floating body effects which are triggered by the impact ionization charging of the film body. However, the kink effect has also been reported previously for long channel bulk Si MOS devices, without buried insulator, in the case of very low temperature operation [1]. This behavior has been attributed to the strong impurity freeze-out which leads to a high substrate resistance in the liquid helium temperature range [1]. A significant substrate current together with a substantial substrate resistance can induce a large forward biasing of the source-substrate diode and, therefore, an important reduction of the threshold voltage leading to an excess drain current in the output $I_d(V_d)$ characteristics. Recently, a kink effect has also been shown in the case of single-drain MOS transistors in the 0.1μm channel length range operated at liquid nitrogen temperature [2]. It has also been reported that, for applied biases in the kink effect regime, it was impossible to measure the impact ionization current at the substrate contact [1,2]. The aim of this work is to study thoroughly the kink effect in a wide temperature range for 0.1μm and sub-0.1μm single-drain (SD) and LDD MOS devices. It is found that the kink effect can be observed even at room temperature for sub-0.1μm bulk Si MOSFETs. On the other hand, it is shown that short channel effects in the deep submicron range are responsible for original kink effect and substrate current variations.

2. RESULTS AND DISCUSSION

Figure 1a shows the variations of the $I_d(V_d)$ characteristics as a function of temperature for a 0.07 μm gate length LDD MOSFET, which leads to an effective channel length in the sub-50 nm range. A significant improvement of the drain current in saturation is obtained in the liquid nitrogen temperature range for gate voltages sufficiently high compared with the threshold voltage. This enhancement of I_d at low temperature, observed for these LDD structures, has been in fact attributed to gate overlapping effects, due to the use of poly-Si side wall spacers, and field assisted impurity ionization in the LDDs [3]. On the other hand, a kink effect is observed in these devices whatever the temperature is, even at 300 K. As it has been mentioned in the introduction, the kink effect was previously reported for low temperature operation, but it is the first time that it is also shown for bulk Si MOSFETs at 300 K with a grounded substrate contact. The kink is observed at this temperature for drain bias lower than 2V, which *highlights the substantial increase of forward biasing effects of the source/substrate diode in the deep submicron range*. This original behavior is attributed to the ultra-short distance between the source and drain regions, the barrier height at the source/substrate junction being strongly influenced by the variation of the potential close to the drain due to the impact ionization current.

In figure 1b are presented the output characteristics in the case of a 0.07 μm LDD MOS transistor, which shows significant short channel effects compared with the previous device of figure 1a, in particular at room temperature, due to a smaller effective channel length. A *significant reduction of the kink effect* is highlighted in figure 1b, for the transistor with substantial short channel effects, compared with Fig. 1a between room and liquid helium temperature. For instance, at 300 K, the kink effect has been suppressed for the device of Fig. 1b. This behavior is observed together with a substantial change of the substrate current. In fact, as it will be shown below, for the MOSFET of Fig. 1b, it is possible to measure a conventional substrate current until high drain bias and low temperature, which is not the case for the device of Fig. 1a.

Similar phenomena have been observed in the case of very short gate length (0.2μm) SD MOSFETs, which leads to effective channel lengths in the 0.1 μm range. Fig. 2 presents the $I_d(V_d)$ characterictics of 0.2 μm gate length single-drain transistors, for devices without (Fig. 2a) and with (Fig. 2b) substantial short channel effects (drain leakage current at high V_d). A significant reduction of the kink effect is also clearly observed for the device of Fig. 2b. This smaller kink effect can be explained by a reduction of the barrier height of the source/substrate junction for the device with substantial short channel effect, due to the strong overlapping of source and drain depletion regions. Therefore, the excess potential induces by the kink effect is limited by this reduced barrier height, and, a lower change of the threshold voltage is thus obtained with increasing V_d. However, this sole barrier height influence cannot explain the following substrate current results.

Fig. 3 shows the substrate current-gate voltage characteristics in the case of a 0.2 μm gate length SD device at liquid nitrogen temperature. For the transistor without short channel effect, flat characteristics are observed for V_d higher than 1.6 V (Fig. 3a). For the MOSFET which shows substantial short channel effects, conventional $I_b(V_g)$ curves are obtained for drain voltages up to 2V (Fig. 3b). Similar effects have been observed for LDD devices (Fig. 4). In fact, in the case of Figs. 3a and 4a, it is not possible to measure the substrate current for high V_d values, due to the strong forward biasing of the source/substrate diode which leads to a *large majority carrier current flow towards the source contact.* Therefore, the substrate current measured at the substrate contact becomes constant versus V_g at the beginning of the strong forward biasing of the source/substrate diode, and flat characteristics are observed instead of the maximum substrate current peak. In the case of the devices which show significant short channel effects, a very different behavior is obtained, with a successful measurement of the substrate current for higher drain biases. This original phenomenon is in fact attributed to two conflicting effects. The forward biasing of the source/substrate diode by the impact ionization majority carrier current leads to an increase of the potential at this junction, but, also induces a substantial reduction of the depletion region under the gate. This last effect seems to be very important for the devices which show significant short channel effects and therefore have a small barrier height at the source/substrate junction, and could lead to a decrease of the potential at this junction. Therefore, a quasi-equilibrium is obtained because of these two conflicting phenomena, inducing, in fact, a *lower increase with V_d of the forward biasing of the source/substrate diode* compared with MOSFETs which show no short channel effect. A *reduction of the kink and a measurement of the substrate current for higher V_d values* are thus observed between room and liquid helium temperatures (Figs. 1-4).

3. CONCLUSION

The kink effect has been thoroughly investigated in a wide temperature range for 0.1μm and sub-0.1μm single-drain and LDD MOS devices. It has been found that the kink effect can be observed even at room temperature for sub-0.1μm bulk Si MOSFETs. On the other hand, it has been shown that short channel effects, observed in the deep submicron range, lead to reduced kink effects and allow to measure the substrate current for high drain biases and low temperatures, due to a lower variation with V_d of the barrier height at the source/substrate junction.

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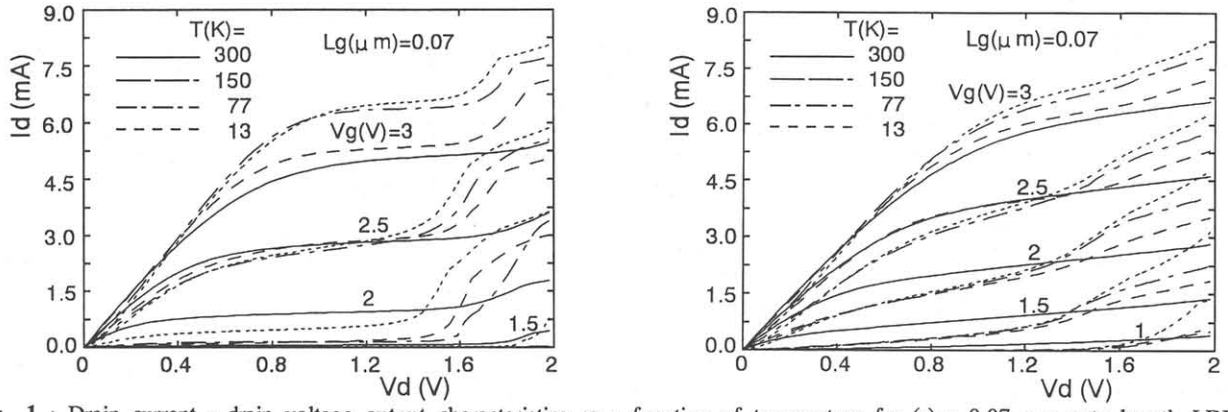

Fig. 1 : Drain current - drain voltage output characteristics as a function of temperature for (a) a 0.07 μm gate length LDD MOSFET's without short channel effect, and (b) a 0.07 μm gate length LDD MOSFET's showing significant short channel effects.

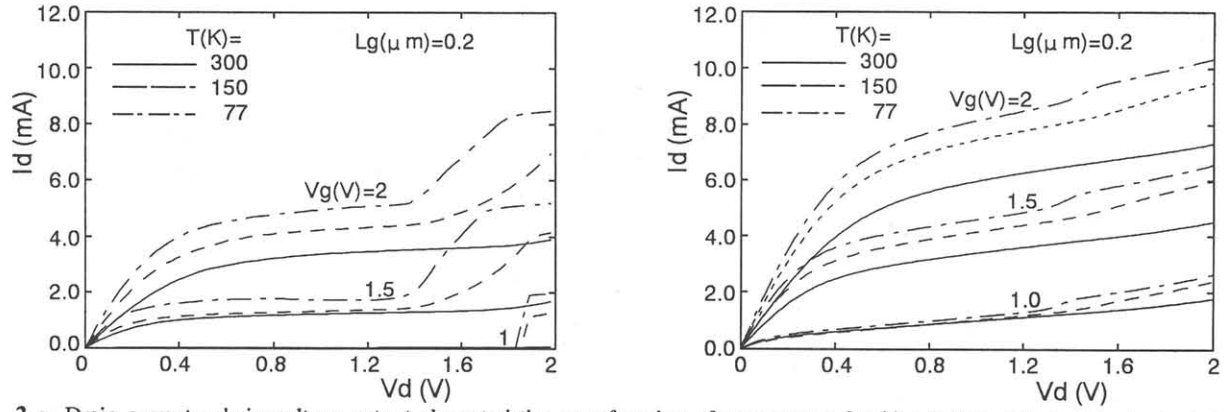

Fig. 2 : Drain current - drain voltage output characteristics as a function of temperature for (a) a 0.2μm gate length single-drain MOSFET's without short channel effect, and (b) a 0.2μm gate length single-drain MOSFET's showing significant short channel effects.

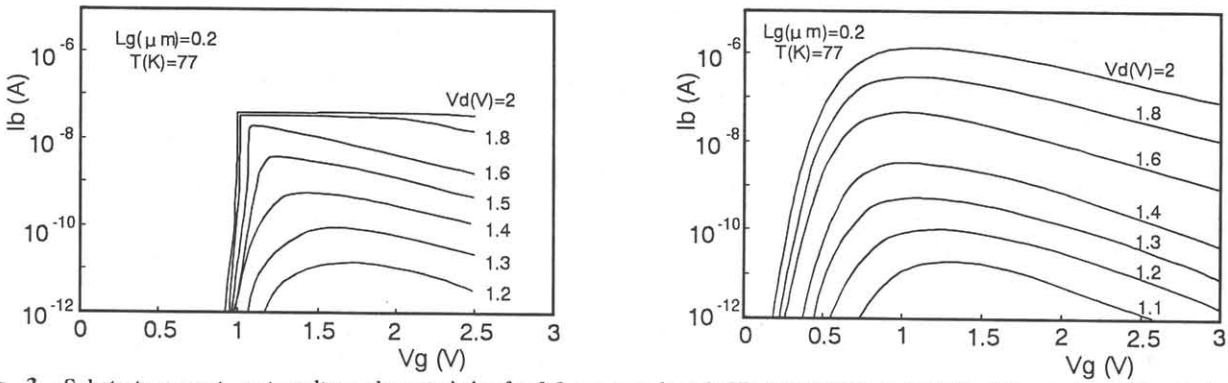

Fig. 3 : Substrate current - gate voltage characteristics for 0.2 μm gate length SD MOSFETs at 77K for (a) a device without short channel effect, and (b) a device which shows substantial short channel effects.

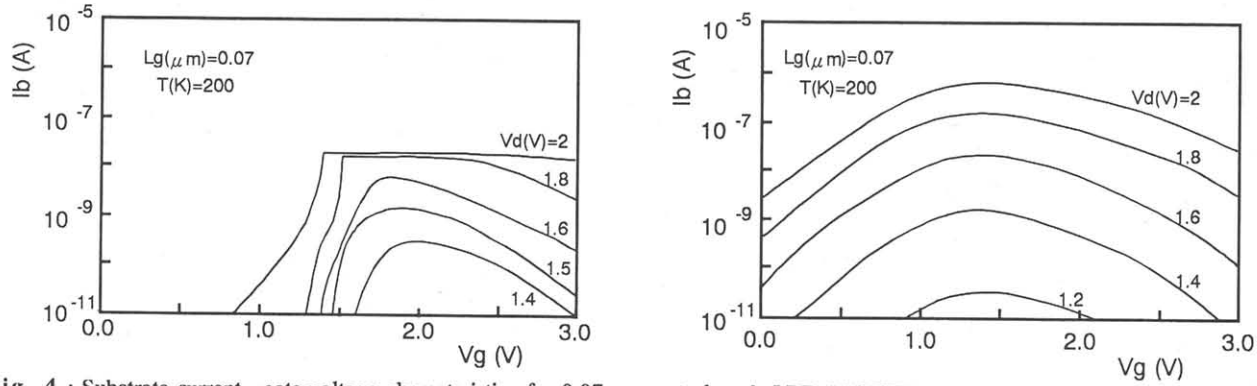

Fig. 4 : Substrate current - gate voltage characteristics for 0.07 μm gate length LDD MOSFETs at 200K for (a) a device without short channel effect, and (b) a device which shows substantial short channel effects.