Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 898-900

A New PMOSFET's Hot-Carrier Degradation Model for Bi-Directional Operation

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We present a new hot carrier degradation model of PMOSFET's for bi-directional operation. This model is based on the trap induced barrier lowering and the channel length modulation due to electron traps in the oxide as well as the mobility modulation due to interface states generation. By extracting the parameters for hot carrier degradation in addition to transistor model parameters, the hot carrier degradation can be predicted not only in the linear and the saturation regions but also in the forward and the reverse operation modes.

1. Introduction

The device degradation due to hot carrier effect has been increasing importance in the long-term reliability of ULSI[1,2]. In scaling down to the deep submicron region, it has been recently recognized that not only NMOSFET's but also PMOSFET's meet the severe restriction due to hot carrier injection which influences a CMOS circuit performance. For PMOSFET's, recently, C.C.Li et al. reported the drain current degradation model[3] based on the concept of channel shortening due to hot carrier. Y.Pan reported the saturation drain current degradation model[4] based on physical parameters on the capture cross section and the density of states of electron traps. In this paper, we will present a new approach to predict the hot carrier degradation for PMOSFET's. A unique feature of our model distinguished from previous reports is based on the trap induced barrier lowering and the channel length modulation due to electron traps in the oxide and the mobility modulation due to interface states generation. Using this model, the degradation on PMOSFET's due to hot carrier injection can be predicted not only in the linear and the saturation regions but also in the forward and the reverse operation modes.

2. Experiments and Modeling

The buried channel PMOSFET's were used with 0.6μm gate length and 8nm oxide thickness to make experiments for modeling and verification. The hot carrier degradation on PMOSFET's is caused by electron trapping in the oxide and the interface state generation[5,6]. Fig.1 shows Vg-Id curves of the initial and the after-stress in the linear and the saturation regions as well as Vg-gm curves. The stress voltages satisfied the maximum gate current condition at Vds=-6.0V. After 10000sec, the shifts were measured in the forward operation mode(FWD) and in the reverse operation mode(REV). For PMOSFET's hot carrier degradation observed are not only the decrease in Vth(ΔVth), the increase in Ids(ΔIds) and the increase in gm but also the difference in shift between FWD and REV. Therefore it is evident that the hot carrier degradation model for bi-directional operation is needed.

Fig.2 shows Vth shift in the linear and the saturation regions for various stress time to distinct this difference. The slope σ(=∂Vth/∂Vds) related to Drain Induced Barrier Lowering(DIBL) in FWD(Fig.2(a)) is the same for various stress time. However, the slope σ(=∂Vth/∂Vds) in REV(Fig.2(b)) changes for various stress time. This phenomena is explained by the Trap Induced Barrier Lowering(TIBL) due to hot carrier induced electron traps at the source end in REV(Fig.3). To include this TIBL effect, ΔVth is divided into the flat band voltage shift(ΔVfb) related to the Vth shift at Vds=0V, and the TIBL shift(Δσ) as given by eq.(1), where the flat band voltage(Vfb) is considered in eq.(2),

$$\Delta Vth = \Delta Vfb + \Delta\sigma \cdot Vds \qquad (1)$$

$$Vfb = \Phi_{MS} + \frac{Qet + Qit}{Cox} \qquad (2)$$

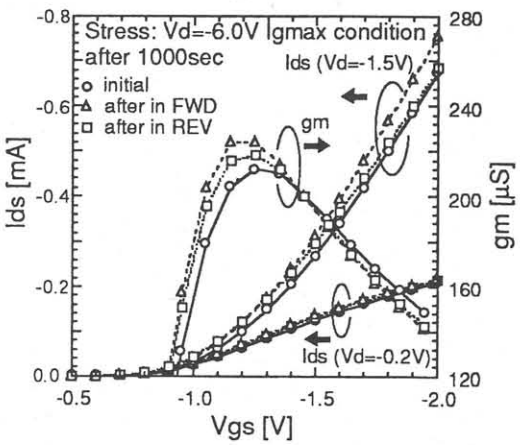
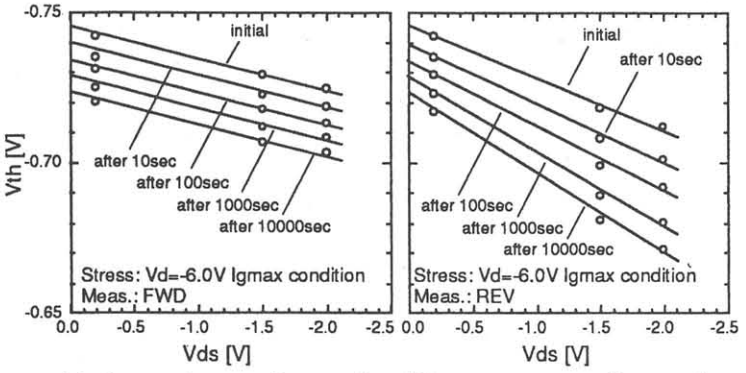
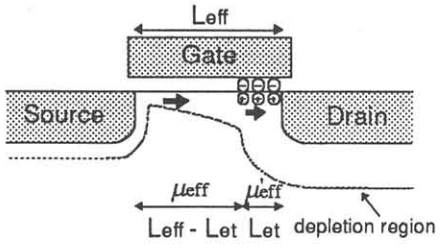


Fig.1 Measured Ids and gm shifts induced by hot carrier compared with the initial in the forward and the reverse operation mode.

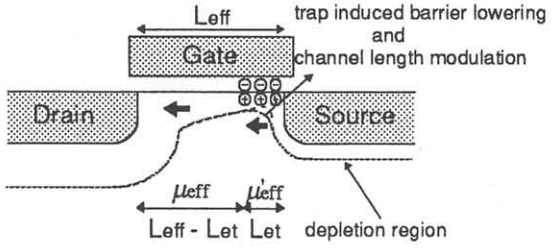


(a) forward operation mode. (b) reverse operation mode.

Fig.2 Vth shifts due to hot carrier effect in the linear and the saturation regions. The slope $\sigma = \partial Vth / \partial Vds$ indicating the DIBL effect, increases as stressing in the reverse operation mode.



(a) forward operation mode.



(b) reverse operation mode.

Fig.3 Trap induced barrier lowering, channel length modulation and mobility modulation effects on PMOSFET's.

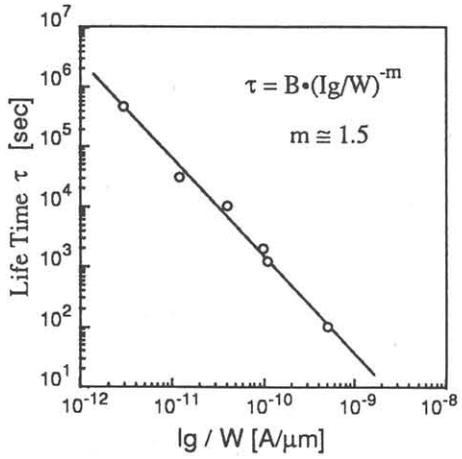


Fig.4 Power law on PMOSFET's hot carrier degradation. Life time τ is defined by flat-band shift; $\Delta Vfb = 10mV$.

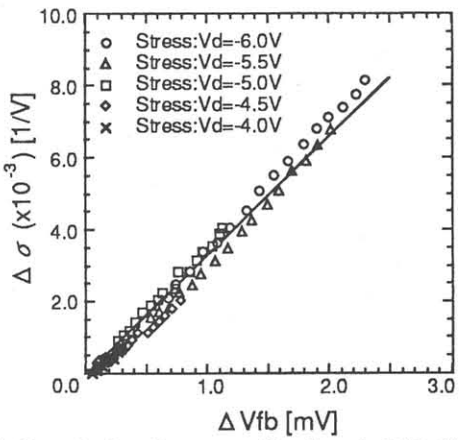


Fig.5 Correlation between flat-band shift (ΔVfb) and TIBL shift ($\Delta\sigma$) in the reverse operation mode at various stress conditions.

where Φ_{MS} is a work function difference, Qet is the effective trapped electron charge density, Qit is the interface state charge density and Cox is the gate capacitance. Hence ΔVfb is reflected by Qet shift(ΔQet) due to oxide electron traps and by Qit shift(ΔQit) due to interface state generation as given by eq.(3).

$$\Delta Vfb = \frac{\Delta Qet + \Delta Qit}{Cox} \qquad (3)$$

From Vth shift at Vds=0V in Fig.2(a) and Fig.2(b), ΔVfb in FWD is observed to be equal to that in REV. Fig.4 shows that the lifetime defined by ΔVfb(Vth shift at Vds=0V)=10mV yields to a power law of hot carrier degradation in eq.(4) introduced by T.C.Ong et al.[7],

$$\tau = B \cdot (Ig/W)^{-m} \qquad (4)$$

where B and m are hot carrier degradation constant. Therefore ΔVfb can be predicted by eq.(4).

Fig.5 shows that $\Delta\sigma$ in REV is in proportion to ΔVfb as given by eq.(5),

$$\Delta\sigma = \begin{cases} 0 & \cdots \text{ in FWD} \\ C_1 \cdot \Delta Vfb & \cdots \text{ in REV} \end{cases} \qquad (5)$$

where C_1 is a constant. This relation comes from the facts that ΔVfb depends on the increase in electron oxide traps(ΔQet) and that $\Delta\sigma$ is related to the barrier lowering by the trapped electron at the source in REV.

The modulation of the effective channel length is also induced by the TIBL. In general, there is the relation between the DIBL coefficient(σ) and the effective channel length(Leff) as expressed by eq.(6),

$$\sigma \propto Leff^{C_2} \qquad (6)$$

where C_2 is a constant. Therefore the relation between $\Delta\sigma$ and modulated channel length(Leff-Let) in Fig.3 is represented by eq.(7).

$$\frac{Leff - Let}{Leff} = \left(\frac{\Delta\sigma}{\sigma} + 1\right)^{1/C_2} \qquad (7)$$

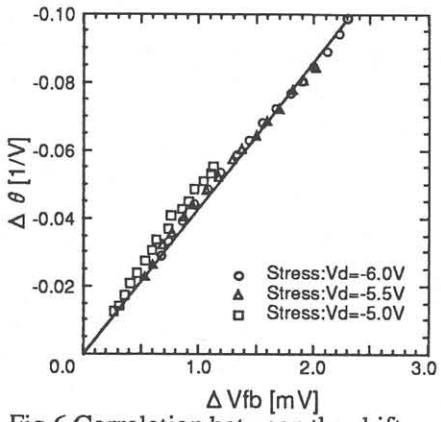
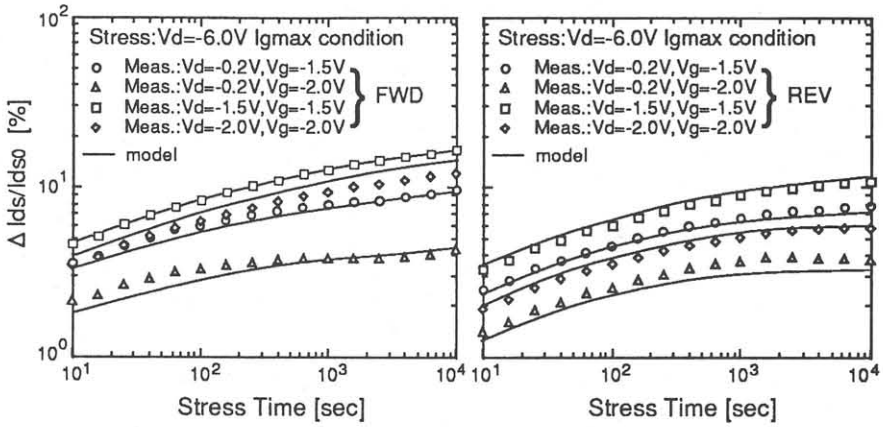


Fig.6 Correlation between the shift on flat-band voltage(ΔVfb) and the shift on vertical electric field dependence of effective mobility (Δθ).



(a) forward operation mode. (b) reverse operation mode.

Fig.7 Comparison between measured Id shift and calculated Id shift by our model.

By using eq.(7) and the measured Δσ, the channel length modulation(Let) can be calculated.

The variation of gm in Fig.1 is found to be due to the increase in the vertical electric field dependence shift(Δθ) for effective channel mobility. Therefore modulated effective mobility(μeff') is expressed in eq.(8).

$$\mu eff' = \frac{\mu_0}{1 + (\theta+\Delta\theta)\cdot(Vgs-Vth)} \quad (8)$$

Fig.6 shows the relation between Δθ and ΔVfb as given by eq.(9),

$$\Delta\theta = C_3 \cdot \Delta Vfb \quad (9)$$

where C_3 is a constant. This relation comes from the facts that ΔVfb is related to ΔQit, which is the interface state charge density, and that Δθ is related to the interface state generation.

Using the above models based on the TIBL effect, the channel length modulation and the mobility modulation, the stressed drain current(Id') due to hot carrier injection is represented by eq.(10) in the linear region and by eq.(11) in the saturation region,

$$Ids.lin' = \frac{Weff\ Cox\ \mu eff'}{Leff - Let + Vds/Esat} \cdot Vd\left(Vgs-Vth_0-\Delta Vth-\frac{Vds}{2}\right) \quad (10)$$

$$Ids.sat' = \frac{Weff\ Cox\ \mu eff'}{Leff-Let-\Delta L+Vds/Esat} \cdot Vdsat\left(Vgs-Vth_0-\Delta Vth-\frac{Vdsat}{2}\right) \quad (11)$$

where Weff is effective channel width, Vth_0 is initial threshold voltage before stress, ΔL is velocity saturation region and Esat is channel field at which the carriers reach saturation velocity.

3. Verification

Fig.7 compares the calculated results by the current model with the measured results for the stressed drain current shift under the maximum gate current stress condition at Vds=-6.0V. The measurement conditions are four ways (in the linear and the saturation regions). Fig.7(a) and (b) show in FWD and in REV, respectively. It should be noted that quite good agreement is obtained. It is confirmed that the good agreement in other various stress conditions(not shown) can be obtained between the measurement and the prediction by our model.

4. Conclusion

We have presented a new approach for PMOSFET's hot carrier degradation model. By extracting the parameters related to hot carrier degradation, the shift can be predicted not only in the linear and the saturation regions but also in the forward and the reverse operation modes. Our model is easily applicable to the bi-directional and dynamic hot carrier simulation for circuit reliability.

5. Acknowledgment

The authors would like to express their thanks to Dr. H. Komiya for their continuous encouragement.

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