

Two-Dimensional Analysis of Interface State Induced Performance Degradation in LDD MOSFET's

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Abstract - We have performed a two-dimensional simulation to analyze the interface trap induced drain current degradation in submicron MOSFET's. Both interface charge incurred conduction charge reduction and mobility degradation are considered. The variation of the drain current in a 0.6 μm LDD MOSFET was characterized in a normal mode and in a reverse mode, respectively, to compare with the simulation. Our study shows that a significant drain current degradation appears in the linear region while the current reduction is only a few percentage points in the saturation region in a normal mode measurement. In a reverse mode, the drain current degradation is significant in the entire region of drain bias.

I. Introduction

As the Si MOSFET technology is moving rapidly into deep submicron domain, hot carrier induced degradation in n-MOSFET's has been identified mainly due to interface trap generation [1,2]. Extensive experimental studies have been conducted not only on the profiling of interface traps [3] but also on their influence on device characteristics [4]. In this work, we have developed a two-dimensional numerical simulation to analyze the interface trap induced performance degradation after hot carrier stress. Our simulation includes an interface state generation mechanism, hot carrier injection and nonuniform reduction of channel electron concentration and mobility due to interface charge. A 0.6 μm LDD MOSFET was stressed at a drain bias of 7V and a gate bias of 3V for 10^4 seconds. The variation of the drain current was characterized in a normal mode and in a reverse mode.

II. Interface Trap Generation Model

Various theories have been proposed to explain the interface state generation mechanism [5,6]. Here, we adopt a breaking Si-H bond model [5]. In this model, hot electron injection is responsible for breaking of the Si-H bond in n-MOSFET's. Subsequently, hydrogen diffusion takes place in the silicon dioxide. The time-dependent interface trap generation rate is therefore determined by the breaking rate and the hydrogen diffusion rate. Thus,

$$\frac{d\Delta N_{it}(x)}{dt} = \frac{AJ_{ch}(x)}{1+B\Delta N_{it}(x)} \quad (1)$$

where x is along the channel direction, ΔN_{it} is the hot carrier stress generated interface state density, A and B

are fitting parameters in the simulation. In the above Eq., $J_{ch}(x)$ is the hot electron injection current across the interface and its calculation can be found elsewhere [7].

III. Drain Current Degradation

Because of the presence of acceptor-type interface states, electrons may be trapped at the interface to form negative interface charge ΔQ_{it} . Consequently, the threshold voltage has a positive shift and the quantity of conduction charge reduces. In addition, an empirical mobility degradation formula [1] arising from Coulomb scattering due to interface charge is also incorporated in the two-dimensional device simulation.

The experimental and simulated drain currents before and after hot electron stress are shown in Fig. 1(a) and Fig. 1(b). Good agreement between experiment and simulation has been achieved with a maximum interface state density of $1.2 \times 10^{12}/\text{cm}^2$ in the simulation. A significant drain current degradation is observed in the linear region. The degradation can be well explained by Fig. 2 where the equi-electron concentration contour with a current flow before and after stress are plotted. Apparently, interface charge (marked by crosses in the figure) results in a decrease of electron concentration underneath and accordingly the current flows deeper in the interface trap region. Fig. 3 shows the sheet conduction electron densities before and after stress. The reduction of conduction charge due to interface traps is more clearly demonstrated in the figure. As a contrast, the drain current degradation in the saturation region is much smaller in a normal mode measurement. The reason is that a channel depletion exists in the n^+ region, where the generated interface states are located, due to a large drain voltage in the saturation region. The low electron quasi Fermi level in the depletion region results in less electron occupation

of interface states. Thus, the effects of mobility degradation and conduction charge reduction are smaller in the saturation region. Fig. 4 shows the variation of the two-dimensional electron concentration distribution after stress and Fig. 5 compares interface charge and the corresponding mobility degradation in the linear region and in the saturation region, respectively. It should be pointed out that no oxide charge induced threshold voltage shift is observed from the drain current characteristics.

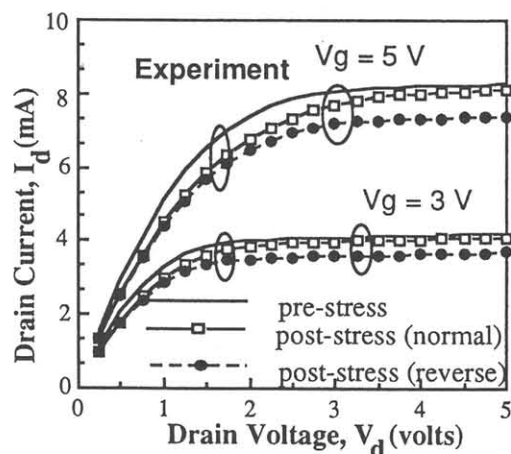
In a reverse mode, the interface state region is always deep in inversion no matter of an applied drain bias. The drain current degradation is appreciable in the entire region of drain bias. Fig. 6 shows the equi-electron concentration contours before and after stress in a reverse mode at $V_g=2V$ and $V_d=5V$. The interface charge and mobility degradation in a normal mode and in a reverse mode are compared in Fig. 7.

Acknowledgements

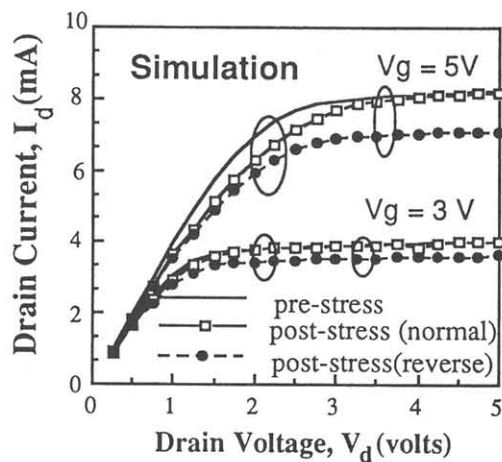
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(a)



(b)

Fig. 1 (a) measured I_d versus V_d characteristics before and after stress. (b) simulated I_d versus V_d characteristics before and after stress.

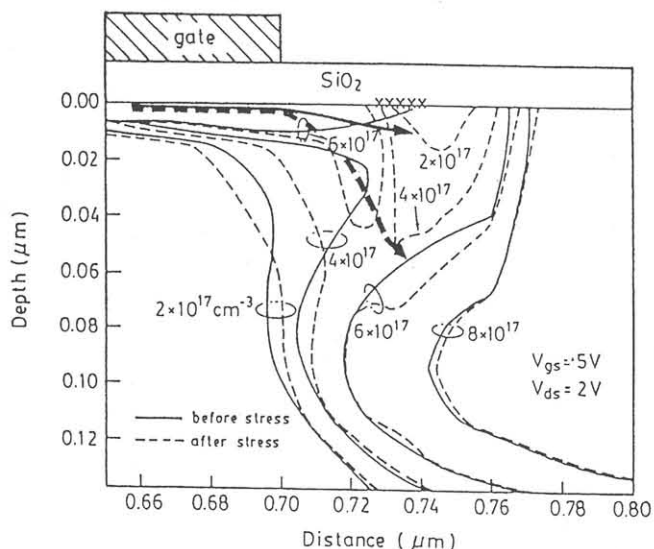


Fig. 2 Simulated 2D distributions of electron concentration before and after stress. Current flows are shown by a thick solid line (before stress) and by a thick dashed line (after stress). Interface traps are marked by crosses.

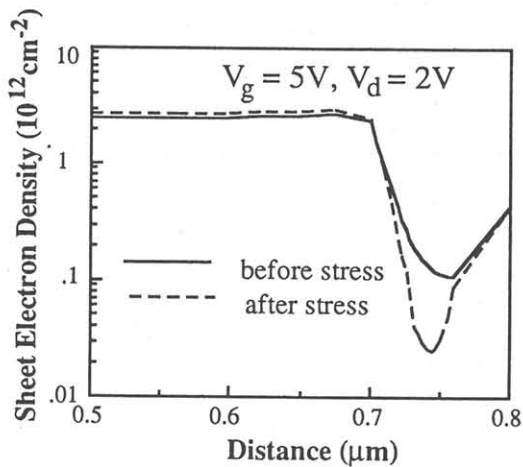


Fig. 3 Sheet electron concentration distributions along the channel before and after a stress at $V_g=5V$ and $V_d=2V$.

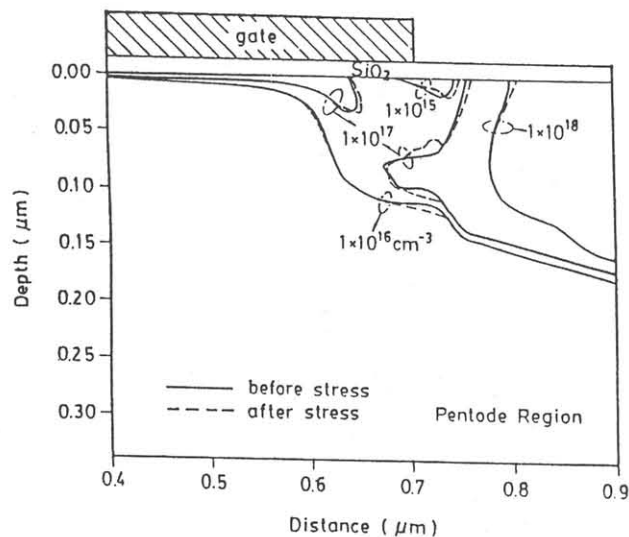


Fig. 4 2D distributions of electron concentration before and after stress in the saturation region.

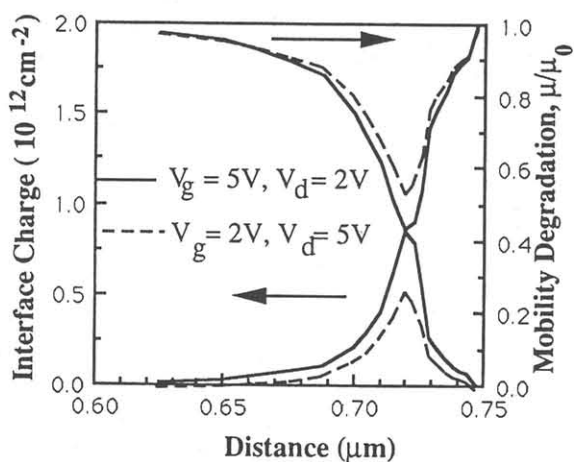


Fig. 5 Interface charge distributions and mobility reductions at $V_g=5V$ and $V_d=2V$ (linear region) and at $V_g=2V$ and $V_d=5V$ (saturation region).

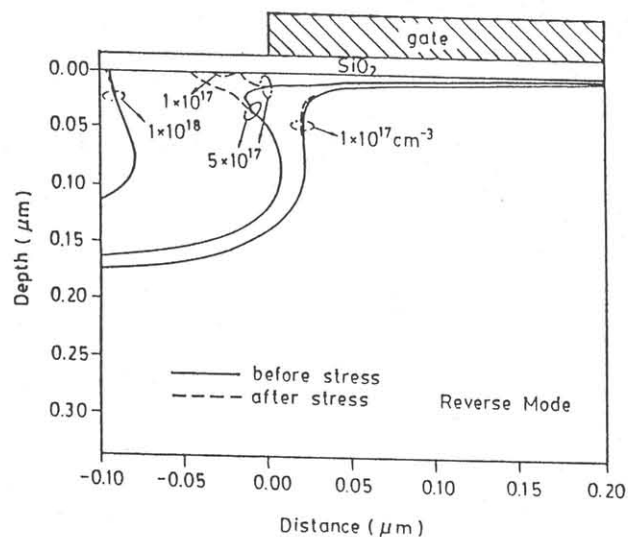


Fig. 6 2D equi-electron concentration contour before and after stress in a reverse mode. $V_g=2V$ and $V_d=5V$.

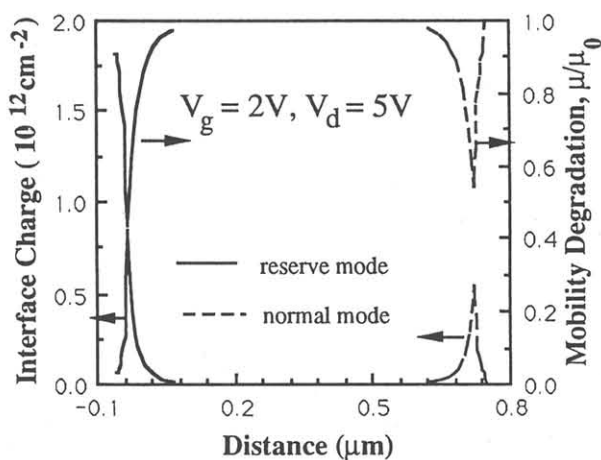


Fig. 7 Comparison of interface charge and mobility degradation in a normal mode and in a reverse mode.