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Analysis of Isolation Degradation Induced by Interlayer Material in Capacitor Over Bit-Line (COB) DRAM Cell

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The isolation degradation in COB DRAMs and the origin of the degradation are described. A lowering of the N-ch field threshold voltage was observed, when the interlayer oxide was TEOSBPSG covered with SiN, corresponding to a capacitor dielectric film. The flat-band voltage shift caused by positive charges at the SiO_2/Si interface was the origin of the threshold voltage lowering. Carbon pileup at the SiO_2/Si interface observed by SIMS analysis is considered to be the origin of the charge. Residual organic compounds in TEOSBPSG migrated to the interface during the thermal treatment process, resulting in the charge.

1.Introduction

As devices are scaled down, requirements for low temperature planarization of interlayer oxides increase. TEOS(Tetraethyl orthosilicate)-based BPSG has been widely investigated for the interlayer oxide because it provides better planarity than SiH_4-based BPSG at the same reflow temperature. Organic compound-based oxides such as spin on glass(SOG) and TEOSBPSG, however, have possibility to degrade device electrical characteristics due to residuals. In truth, it has been reported that SOG brought about the field inversion in MOS devices[1]. It was explained that the origin of the inversion was due to the interaction of residual organic compounds in SOG with H evolved from cap plasma silicon nitride film.

In this study, the influences of TEOSBPSG on capacitor over bit-line(COB) DRAM (Fig.1) is reported. The COB structure is the most promising cell structure for high density DRAMs beyond 64M, because it can enlarge the capacitor area using a three-demensional capacitor structure[2].

Isolation degradation was observed in some COB DRAM cells so to investigate the origin of this problem, the influences of the SiN film and interlayer dielectric films were examined. Only the combination of the SiN film and interlayer TEOSBPSG showed a degradation in isolation characteristics. It is also shown that positive charges at the SiO_2/Si interface lowered the field threshold voltage and the positive charges are probably due to carbon pileup at the interface.

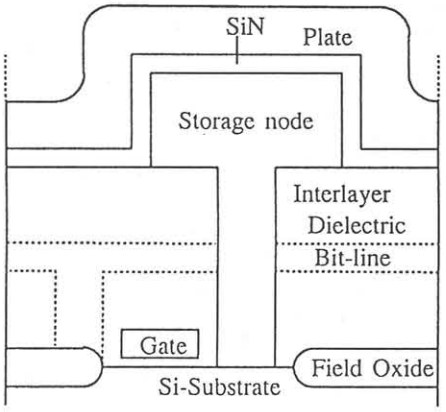

Fig.1 Schematic cross-section of the COB (Capacitor Over Bit-line) DRAM cell structure.

2.Experiments

Al-gate parasitic field transistors and field MOS diodes were fabricated to evaluate the influence of interlayer material and SiN. These devices consisted of the following common interlayer dielectric structure, as shown in Figs.2 and 3. The thicknesses of field oxide, interlayer film and SiN film were 350nm, 300nm and 10nm, respectively. The SiN thickness corresponds to that for the DRAM capacitor dielectric film. The SiN film was deposited by low-pressure chemical vapor deposition (LPCVD) from SiH_2Cl_2 and NH_3. Some specimens lacked the SiN film for comparison. LPCVD TEOSBPSG and SiH_4-based BPSG, PSG, BSG and undoped SiO_2 were used as interlayer

films. TEOS was used as a source gas for TEOSBPSG, and SiH_4 was used for BPSG, PSG, BSG and undoped SiO_2. Some specimens were annealed at 850°C for 30min after formation of these films, similar to the typical DRAM fabrication process.

The field threshold voltage of the Al-gate field transistor was measured by ramping the gate and source voltage together untill the drain current increased to 1μA for the 50μm-width field transistors. The flat-band voltage shifts (ΔV_{fb}) of the field MOS diodes were obtained by high frequency C-V measurement at 10MHz. Some specimens were analyzed by secondary ion mass spectrometry (SIMS).

3.Results and Discussion

Figure 2 shows the field threshold voltage of the N-channel Al-gate field parasitic transistors. The interlayer film was TEOSBPSG. The specimen without the SiN film shows no threshold voltage lowering until the isolation is narrowed to 0.4μm which is the typical design rule of 64M DRAM. On the other hand, the specimen covered with the SiN film shows lowering at 0.7μm. Typical of COB DRAMs, MOS devices are fully covered by the SiN film, as shown in Fig.1, which is different from bit-line over capacitor and trench capacitor structures. Therefore, this phenomena is peculiar to COB DRAMs.

To investigate whether this isolation degradation originated from the field inversion or not, the MOS diodes were evaluated by C-V measurements. Figures 3 and 4 show ΔV_{fb} obtained by the C-V measurement. The specimen with an undoped SiO_2 interlayer film is the reference for ΔV_{fb}. Among several kinds of interlayer films, as shown in Fig.3, only TEOSBPSG shows a large ΔV_{fb}. Moreover, even if the interlayer film was TEOSBPSG, the specimens without the SiN cover or annealing show negligibly small ΔV_{fb} as shown in Fig.4. Therefore, the origin of the isolation degradation was the large ΔV_{fb} observed only when the specimens with TEOSBPSG were covered by SiN and annealed.

To investigate the origin of such large ΔV_{fb}, the interlayer dielectrics were gradually etched with dilute HF solution while monitoring the V_{fb} variation and remaining dielectric thickness [3], as shown in Fig.5. V_{fb} decreased in proportion to the reduction of dielectric thickness, which means that positive charges at the SiO_2/Si interface brought about the V_{fb} shift.

Composition analysis by SIMS was performed, and the obtained depth profiles are shown in Fig.6. The specimens of Fig.6(a) and (b) were annealed at 1000°C (ΔV_{fb}>-35V) and 850°C (ΔV_{fb}=-23.4V), respectively, and that of Fig.6(c)

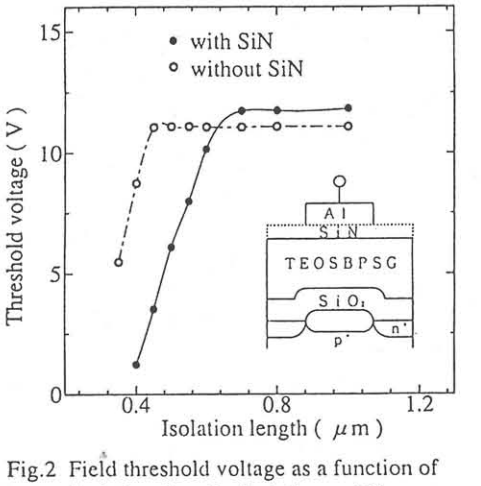

Fig.2 Field threshold voltage as a function of isolation length. Isolation width was 50 μm. All specimens were annealed at 850°C for 30min.

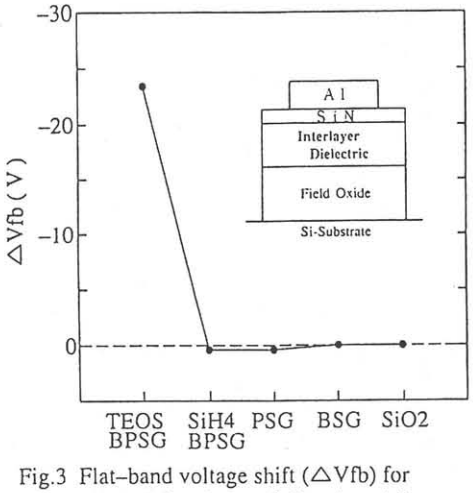

Fig.3 Flat-band voltage shift (△Vfb) for several interlayer dielectrics. All specimens were annealed at 850°C.

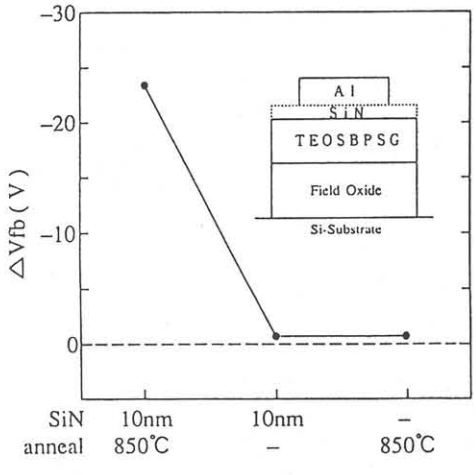

Fig.4 The influence of the SiN film or annealing on the flat-band voltage shift (△Vfb).

was not annealed (ΔV_{fb}=-0.7V). Carbon pileup at the interface is apparent. The amount of carbon pileup increases as the annealing temperature increases. ΔV_{fb} also increases with annealing temperature. There is no great difference between SIMS profilings for Si, O, P of these specimens. These results indicate that the piled-up carbon is the origin of positive charges at the interface.

The speculated phenomenon is shown in the diagram of Fig.7. In the specimen with the TEOSBPSG interlayer film covered by SiN, during the high-temperature thermal treatment process residual organic compounds in TEOSBPSG migrate to the SiO_2/Si interface. These migrated organic compounds result in positive charges there which cause the V_{fb} shift and the N-channel isolation degradation.

4.Conclusion

The origin of isolation degradation in COB DRAM was investigated. The flat-band voltage shift caused by positive charges at the Si/SiO_2 interface lowered the field threshold voltage. The lowering was observed when the interlayer TEOSBPSG was covered with SiN corresponding to the capacitor dielectric film. The carbon pileup at the SiO_2 /Si interface was observed in such specimens using SIMS analysis. During the high-temperature thermal treatment process, the residual organic compounds in the SiN-covered TEOSBPSG are speculated to migrate to the interface, resulting in positive charges.

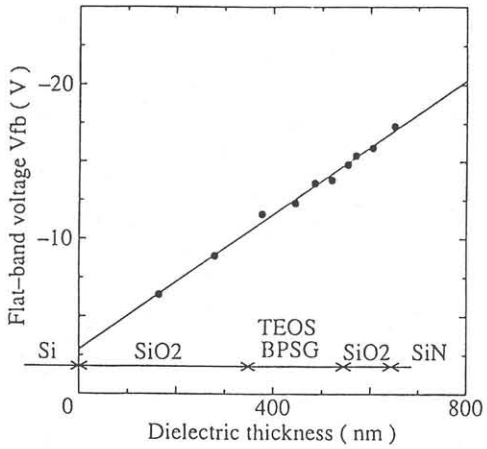

Fig.5 Vfb as a function of remaining dielectric thickness after etching with HF solution for annealed SiN/TEOSBPSG/SiO2.

Acknowledgments

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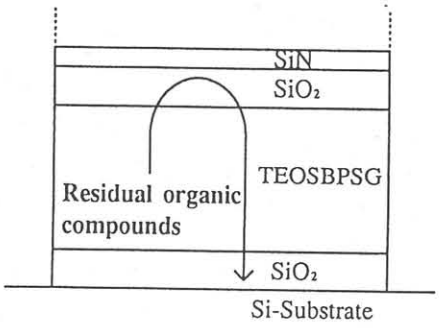

Fig.7 Diagram indicating the speculated C migration to the SiO_2 /Si interface.

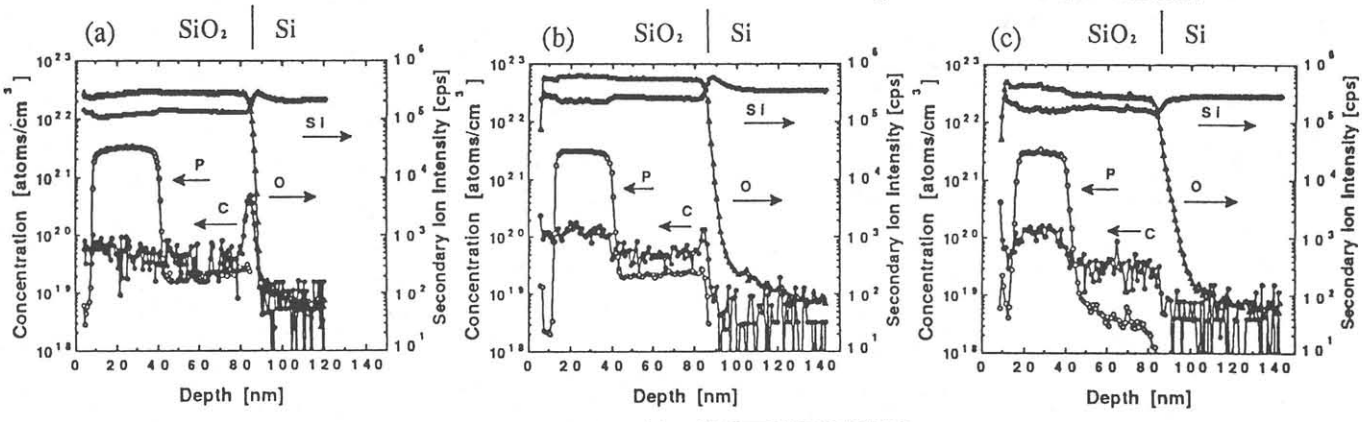

Fig.6 SIMS profiles of P, C, O, Si for SiN/TEOSBPSG/SiO_2
(a) with annealing at 1000℃ after SiN formation. △Vfb＞-35V.
(b) with annealing at 850℃ after SiN formation. △Vfb＝-23.4V.
(c) without annealing. △Vfb＝-0.7V.