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A 0.4μm Gate-All-Around TFT (GAT) Using a Dummy Nitride Pattern for High Density Memories

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We propose a novel process of double-gate TFT named Gate All-Around TFT (GAT). Device process is very simple in which we realize double-gate structure using only a dummy nitride pattern. The GAT shows high channel conductance peculiar to the double-gate structure. It can also eliminate a anomalous leakage current which appears in the sub-half micron regime. Combining with a sacrifice oxidation of the channel poly-Si, we obtained the excellent performance GAT.

1. Introduction

TFT's are key devices for high density SRAMs and LCDs. In order to achieve high performance of TFT, double-gate structure has been proposed for TFT's [1][2][3], and SOI-MOSFETs [4]. Since the channel has two gate electrodes not only on the channel but also underneath it, twice width of channel and the volume inversion improve the TFT performance remarkably. Moreover, the double-gate structure makes it possible to stack TFT's near the external conductive layers, because the channel poly-Si is shielded by the double gates. Therefore, the height of memory cell can be suppressed by thinning of the interlayer dielectric films. Recently, GAA (Gate-All-Around) structure for SOI devices was proposed to eliminate this obstruction, in which both gate poly-Si and gate oxide are fabricated simultaneously [5]. Although this attractive structure can be applied to TFT process, it has a serious problem to utilize for high density SRAMs. The problem is that the bottom gate length in GAA process is determined by the wet etching, and so this process is unsuitable for sub-half micron devices.

In this paper, we propose a novel TFT structure with a gate surrounding the channel, which is named Gate-All-Around TFT (GAT) . We can realize simple fabrication process of GAT structure using a dummy nitride pattern.

2. Device Fabrication

Figure 1 shows the fabrication process of GAT. At first, 100 nm-thick silicon nitride film is deposited on oxidized Si wafer and is patterned. This pattern is named a dummy nitride pattern. Channel poly-Si pattern is fabricated across this dummy nitride pattern by the a-Si deposition, its crystallization and patterning as shown in Fig.1(a). The thickness of the channel poly-Si is 80 nm. Then, the nitride pattern is fully removed by hot phosphoric acid. As a result, the channel poly-Si, which had been located on the dummy nitride pattern, floats in the air like a bridge, as shown in Fig.1(b). This process step is the key point of the GAT structure. Gate oxide and gate poly-Si are deposited by LP-CVD on this wafer. The thickness of the gate oxide and gate poly-Si are 15 nm and 150 nm, respectively. Since the coverage of LP-CVD is excellent, the gate oxide and gate poly-Si are deposited all around the channel poly-Si, as shown in Fig.1(c). The gate poly-Si is phosphorus doped poly-Si. The GAT process, in which top and bottom gate length are determined by the patterning of the gate poly-Si layer and the width of the dummy nitride pattern, respectively, is suitable for sub-half micron regime and beyond. For the comparison, we also fabricated top-gate TFT's as single-gate TFT. Both TFT's are p-channel type and minimum gate length is 0.4 μ m.

3. Results and Discussion

Figure 2 represents the SEM micrograph of the GAT cross section in the direction of channel width. This figure indicates that the dummy nitride pattern underneath the channel poly-Si pattern was fully removed by the phosphorus acid. This figure also demonstrates that the gate oxide and gate poly-Si film surround the channel poly-

Si pattern perfectly and the GAT structure can be realized by this process. In addition to this SEM observation, we verified the GAT structure by means of the electrical measurement. The result shows that the leakage current due to the negative substrate bias is suppressed in the GAT compared to the single-gate TFT. The drooping of the bridge-shape channel poly-Si was not found in the sub-micron gate length. These facts imply that the GAT process is realistic and is not tricky to obtain the gate-all-around structure.

Figure 3 shows the Id-Vd characteristics of p-ch GAT and single-gate TFT. The GAT has large ON-current of 10 μA order and it is about twice as large as that of the single-gate one. Breakdown voltage of both TFT's are larger than 8V. The channel conductance (gm) is shown as a function of Vg in Fig.4. The GAT has superior characteristic of gm especially in low Vg. We consider that the improvement of ON-current mainly results from double channel width, as presented in other double-gate TFT's [1-5]. The gm in higher Vg is, however, lower than the twice of that of the single-gate TFT. Two mechanisms can be estimated to elucidate this reduction. One is a degradation of drain current by parasitic resistance. This GAT has large drain current of 10 μA order, so that the contact resistance and wiring resistance of source and drain poly-Si layer are thought to drop the drain bias. The other is the poor crystallinity of the bottom surface of channel poly-Si. In the crystallization of a-Si film, the crystalline nuclei are generated at the bottom surface. It is considered that there exist a lot of fine grains at the bottom surface as compared to the top surface. Accordingly, the mobility at the bottom surface of the channel poly-Si is probably inferior to that at the top surface, so that the total gm is thought to be lower than the twice of that of the top surface.

Figure 5 shows the Id-Vg curves of 0.4 μm channel length TFT's. In the single-gate TFT, a large leakage current is observed. Since this current becomes prominent as the gate length shrinks, it is considered that the current is punch-through or parasitic MOS current flowing at the back surface. This figure demonstrates that the GAT can reduce the leakage current remarkably. This is because the gate poly-Si covering all around the channel poly-Si fully controls the channel potential of all poly-Si surface.

In order to suppress leakage current further, we utilized a sacrifice oxidation of the channel poly-Si for the GAT structure. After the crystallization of a-Si film, the channel poly-Si was oxidized at 820 ℃ in wet-O2 ambient and then the oxide layer was removed. Figure 6 shows the performance comparison of 0.6 μm GAT with and without the sacrifice oxidation. It indicates that the oxidation process can reduce the leakage current drastically. Moreover, it enhances the ON-current and improves the subthreshold swing. Some papers reported that the performance improvement by the oxidation of channel poly-Si was due to the elimination of the crystalline defects in the poly-Si grain [6X7]. Other report said the double gate effect is very sensitive to the channel poly-Si thickness (2). We speculate that the performance improvement of the GAT with the sacrifice oxidation is caused by the thinning effect of channel poly-Si in addition to the crystallinity improvement. Figure 7 shows the excellent performance of the 0.4 μm GAT with the sacrifice oxidation. The ON-current and subthreshold swing are equal to 24 μA and 73 mV/dec., respectively, and the leakage current is less than 400 fA. These characteristics is close to that of single-crystalline MOSFETs, so that SRAM cell with the GAT has the possibility of showing the good performance as well as that of the full-CMOS cell.

4. Conclusion

We conclude that the GAT process using dummy nitride pattern can realize the double-gate structure with only one additional mask as compared with the single-gate process. Moreover, the sub-half micron TFT, which has the excellent performance, was obtained by the GAT process with the sacrifice oxidation of channel poly-Si. This attractive GAT structure can be employed for high density memories.

5. Acknowledgment

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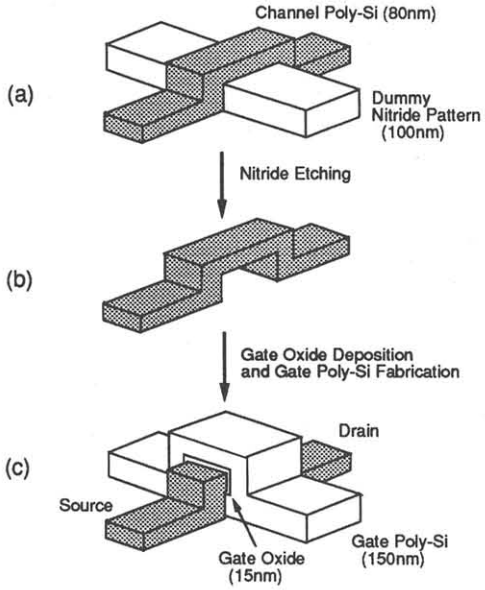

Fig.1 Fabrication process of GAT

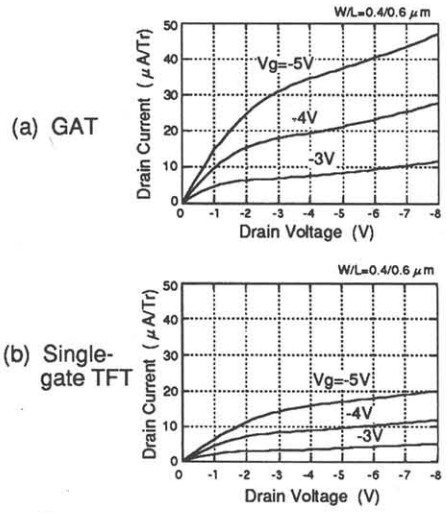

Fig.3 Id-Vd characteristics of GAT and Single-gate TFT. GAT has twice ON-current of that of Single-gate TFT.

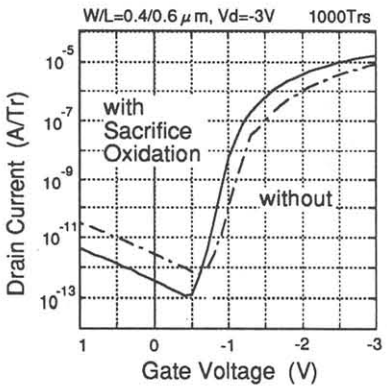

Fig.6 Improvement of sacrifice oxidation for GAT.

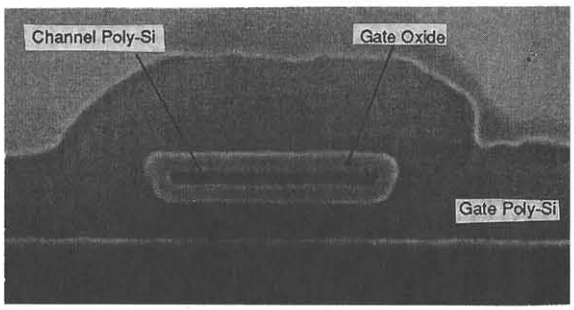

Fig.2 Cross-sectional SEM micrograph of the channel region of the GAT, perpendicular to the current flow direction.The LP-CVD coverage is excellent.

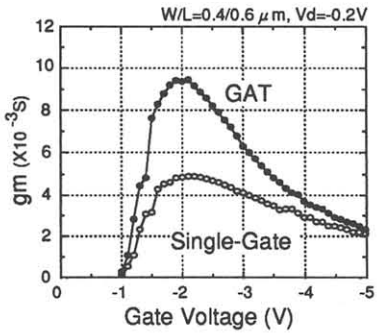

Fig.4 Channel conductance (gm) as a function of Vg. GAT shows superior conductance.

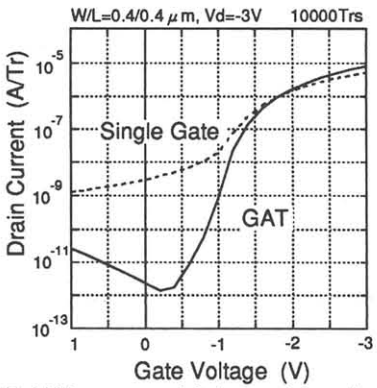

Fig.5 Id-Vg curves of 0.4 μm channel length TFT. GAT suppresses the leakage current.

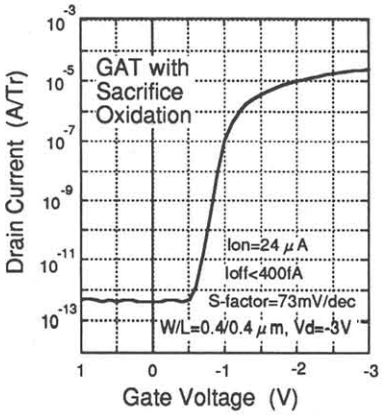

Fig.7 Excellent performance of 0.4 μm channel GAT with sacrifice oxidation.