Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 910-912

A Novel Source-Side Injection Split-Gate Flash Cell Technology for High Density Low Voltage Applications

Yoshimitsu YAMAUCHI, Masanori YOSHIMI, Kiyosige OMORI, Shinji NITTA,
Norio MIZUKOSHI and Katsunori SUZUKI

1st Development Dept., VLSI Research Laboratory, Sharp Corporation
2613-1, Ichinomoto-cho, Tenri-shi, Nara 632, Japan

A novel source-side injection split-gate Flash cell with a self-aligned off-set source (SOS) is proposed for high density low voltage applications. The SOS split-gate cell makes it possible to realize not only 5V-only but also 3.3V-only programming by improving further the programming efficiency of source-side injection cells. This cell is suitable for low voltage read-out due to its no-overerase structure. A small cell area of 3.6μm^2 with 0.6μm technology acceptable for 16Mb Flash is also obtained.

INTRODUCTION

The conventional single gate cell makes it difficult to realize both single power supply programming due to its low programmability and low voltage read-out due to its overerase structure. Recently, several studies [1],[2] on source-side-injection Flash cells have been reported to improve the above-mentioned issues without increasing the cell area. However, they suffer from the high resistance of the side-wall select gate working as a word-line[1] or overerase issues[2].

This paper describes a SOS split-gate cell acceptable for 5V-only or 3.3V-only high density Flash memories.

CELL STRUCTURE

The source-side injection SOS split-gate cell uses a triple level polysilicon (double poly-Si and single polycide) CMOS process, as shown in Fig.1. The cell has a self-aligned stacked memory transistor (MT) with tunnel oxide (100Å) and interpoly ONO (200Å (effective)). The MT gate consists of a floating gate (FG) and a programming gate (PG). The MT has a drain (D) and a self-aligned off-set source (SOS) formed without increasing cell area due to mis-alignment. The cell has no deviation of the off-set channel length (Loff). The select-gate (SG) working as word-line is formed by polycide (WSix/polySi) to reduce its resistance. The gate spacer is made by an ONO stacked film.

A cell area, as small as a conventional single gate cell (3.6μm^2), was realized with a 0.6μm rule by using the SOS (self-aligned off-set source) technology and contactless memory array structure.

The key process steps for the SOS split-gate cell technology are shown in Fig.2. The MT gate was formed followed by the drain implant (Fig.2(a)). The thin ONO gate spacer was formed on the side-wall of the MT gate by etch-back process of the SiN/SiO_2 films and by gate oxidation. Then thin poly-Si(1000Å) was deposited (Fig.2(b)). Next, SiO_2 spacer (0.4μm width) formed followed by phosphorus implant through the thin poly-Si(Fig.2(c)). The WSix film was deposited after removing the SiO_2 spacer, followed by WSix/poly-Si etching to define the SG and peripheral gate (Fig.2(d)). The field area is covered by thin poly-Si during SiO_2 spacer removal that prevents the field threshold decrease by field oxide thinning.

The contactless memory array structure is used to reduce the cell area as shown in Fig.3. The contactless array is realized by using buried N+ diffusion under the field as the drain-line, as shown in Fig.4, to avoid the Si pitting on the drain-line in stacked MT-gate and SG etching. The buried N+ diffusion was formed by arsenic implant followed by field oxidation after high temperature annealing to reduce its junction leakage.

OPERATION PRINCIPLE

Typical operating conditions are shown in Table1. The SOS split-gate cell is programmed by the high efficiency source-side-injection of channel hot electrons and is erased by F-N tunneling. In a program operation, high voltage is applied to the programming gate without suffering from gate-disturb by applying Vcc to the drain. The cell has a select gate, that eliminates the over-erase issue. In addition, the soft-write issues and drain disturb in read operations are also eliminated by applying Vcc to the PG and reading from the off-set source. This operation principle is suitable for low-voltage programming and read-out.

CELL CHARACTERISTICS

The off-set length (Loff) effect on the programmability was evaluated for a source-side injection split-gate cell as shown in Fig.5. The cell shows higher programmed Vt with a shorter Loff due to higher channel current. The programmed Vt remarkably increased with decrease of the Loff for a 3.3V operation.

The SOS split-gate cell with a short Loff of 0.4μm without suffering from the Loff deviation shows high efficient programming characteristics as shown in Fig.6 and Fig.7. The cell is programmed in 1μsec. and 50μsec. for 5V-only and 3.3V-only operations, respectively, and the channel current in programming is as small as 10μA. The cell with these cell characteristics is acceptable not only for a 5V-only operation but also for a 3.3V-only operation by programming multiple memory cells (such as 256 byte) on the same word-line simultaneously.

The cell with depletion-type MT (typical erased Vt=-1V) shows high read current of 180μA (80μA) by applying the low voltage of Vcc to the word-line (SG) for a 5V-only (3.3V-only) operation, as shown in Fig.8.

CONCLUSIONS

The source-side injection SOS split-gate cell realizes fast programming speed of 1μsec. for 5V-only operation and makes it possible to realize 3.3V-only operation by programming multiple memory cells. The cell eliminates the over-erase issues and a small cell area of 3.6μm^2 acceptable for 16Mb Flash is also obtained by using 0.6μm technology.

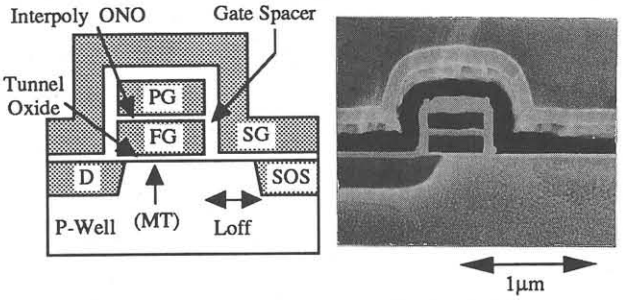
The newly developed SOS split-gate Flash cell technology is suitable for high density low voltage applications.

ACKNOWLEDGEMENT

The authors would like to thank Mr.A.Kagisawa, Mr.T.Sakurai and Mr.R.Miyake for their continuous encouragement during this work.

REFERENCES

[1]K.Naruke et al., IEDM Tech. Dig., pp.603-606,1989.
[2]Y.Yamauchi et al., IEDM Tech. Dig.,pp.319-322,1991.



(a) Schematic View (b) SEM View

Fig.1 The SOS split-gate cell structure.

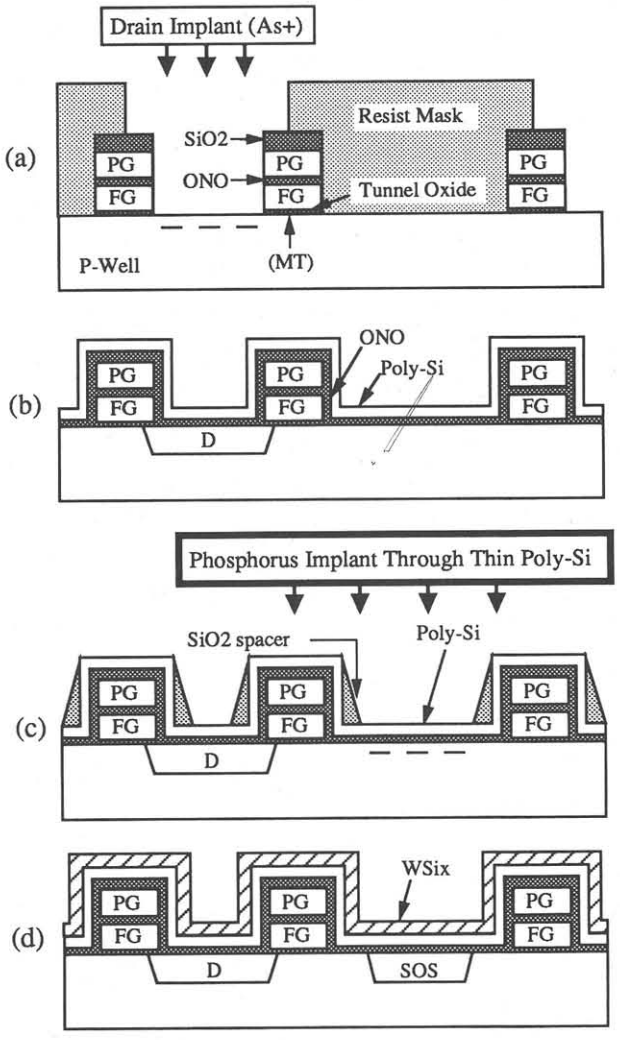


Fig.2 Key process steps for the SOS split-gate cell.

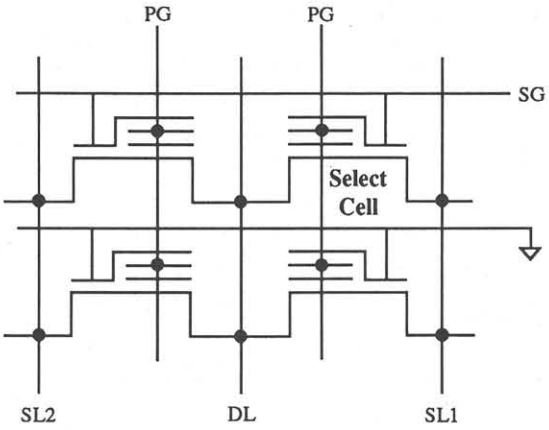
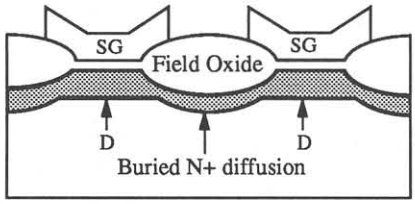
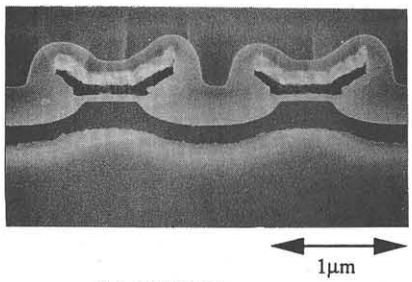


Fig.3 Contactless memory array.



(a) Schematic View



(b) SEM View

Fig.4 The cross-sectional view along Drain-Line of the SOS split-gate cell.

Table 1 Typical operating conditions for 5V-only (3.3V-only).

MODE	DL	SL1	SL2	PG	SG
PROGRAM	5V (3.3V)	0	5V (3.3V)	13V	1.2V
ERASE	5V (3.3V)	FLOAT	FLOAT	-10V (-12V)	0
READ	0	3V (2V)	0	5V (3.3V)	5V (3.3V)

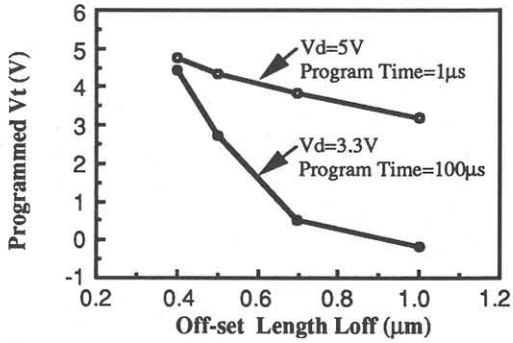


Fig.5 Off-set length (Loff) effect on the program characteristics.

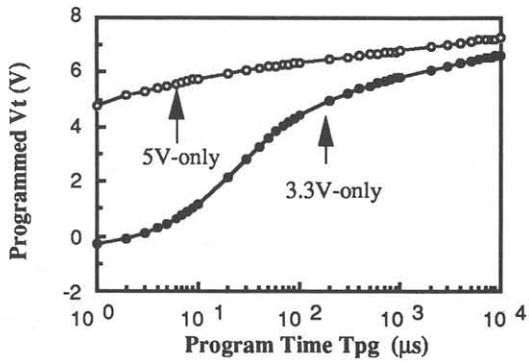


Fig.6 Program characteristics of the SOS split-gate cell.

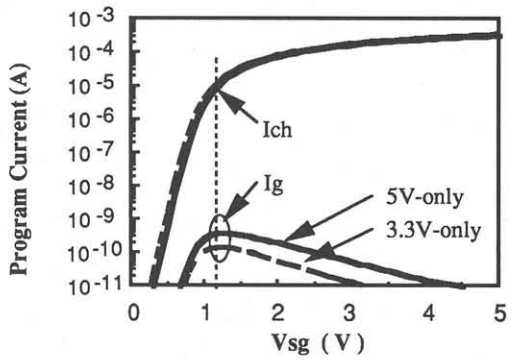


Fig.7 Programming channel current (Ich) and gate current (Ig) of the SOS split-gate cell with contacted floating gate.

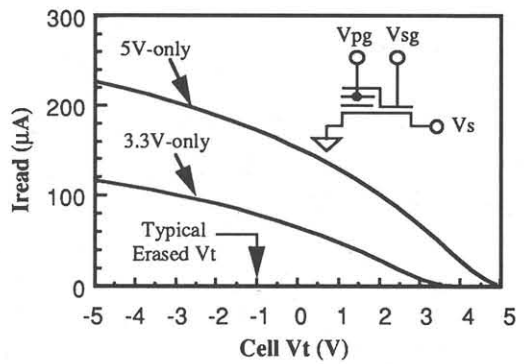


Fig.8 Read current (Iread) as a function of the cell Vt.