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256 Mbit High Density CMOS Non Volatile Memories Field Isolation by Using High Temperature Poly Buffer LOCOS(HTPBL)

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This paper presents the optimization of High Temperature Poly Buffer LOCOS (HTPBL) isolation for 0.25µm design rules CMOS Non Volatile Memories of the 256 Mbit generation. **For the first time,** the characterization of HTPBL in the range 1000°C to 1140°C is reported. The impacts on bird's beak value and shape, 7nm gate oxide defect density and QBD, high voltage sustaining 0.25µm active devices and 0.9µm pitch field isolation are reviewed.Without high energy implanted wells, a 5V holding voltage latch-up resistant 2 µm n+/p+ distance can be achieved with 1100°C HTPBL. The Steam Oxidation Enhanced Diffused Twin Wells architecture and process can be extended to the Gigabit generation.

1.INTRODUCTION

Poly Buffer LOCOS isolation suffers from field oxide thinning[1][2],corner encroachment enlargment [2][3], microtrenching defects induced during buffer silicon removal if low temperature field oxidation is used[2],[4]. High temperature field oxidation will help to solve these problems.

2.PROCESS DETAILS

In the first process step, preannealing of the wafers is achieved in order to improve gate oxide defect density and avoid stacking faults: the specific differences between Czochralski grown silicon and epi have been taken into account whenever these materials are used[5]. The wells drive is performed at 1160°C for field oxidation temperature lower or equal to 1050°C. A low temperature dopant activation is performed if field oxidation temperature is higher than 1100°C. The masking stack is 10 nm pad oxide(SiO2), 60 nm amorphous silicon(a-Si) and 180nm nitride(Si3N4) depositions. Deep U.V. lithography is used for all critical levels.Whether the amorphous silicon (a-Si) buffer layer is etched(Total Stack Etch TSE PBL) or not (Nitride Only Etch NOE PBL) before field oxidation will affect isolation planarity and voltage sustaining. TSE PBL is achieved by a double step stack etch that avoids trenching in small isolation gaps. After field oxidation, mask removal is performed using several steps wet chemistry for SiON and Si3N4 removals and dry HBr,Cl2 based process for a-Si removal.Threshold adjusts and NMOS Boron field are implanted through a high temperature sacrificial oxidation[5]. After sacrificial oxidation strip, a 7 nm O2+HCl gate oxide is grown at 850°C.

3. MORPHOLOGY. ELECTRICAL WIDTH.

Figures 1a &b show SEM cross sections of 1 µm pitch arrays after a 500nm steam field oxidation at 1100°C in the NOE PBL and TSE PBL cases

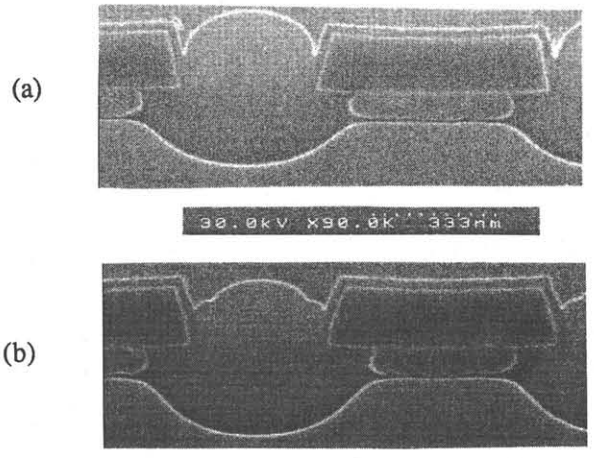
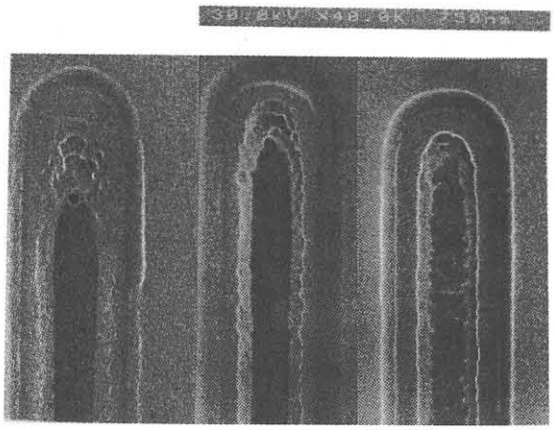


Figure 1 SEM cross section of 1µm pitch array steam oxidized at 1100°C Poly Buffer LOCOS : (a) NOE PBL ; (b) TSE PBL

respectively. Figures 2a,b and c show SEM top views of 0.25µm patterns after field oxidation at 1050°C, 1100°C and 1140°C respectively. Microtrenching is visible at 1050°C and disappears when reaching 1100°C because of pad oxide/substrate interface stress relaxation. Still, at 1140°C the pattern size control will be difficult because of the enhanced diffusion of oxygen at the buffer recrystallized silicon grain boundaries (figure 2c). A correlation is established with the bird's beak values and the dispersion of electrical channel width extracted from narrow channel transistors

transconductance measurments(figure 3).



(a) (b) (c)

Figure 2 SEM top view of 0.25μm TSE PBL finger pattern for different field oxidation temperatures: (a)1050°C; (b)1100°C (c) 1140°C

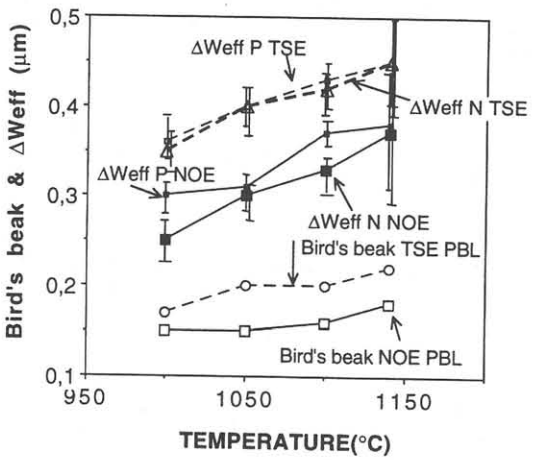


Figure 3 Bird's beak and NMOS,PMOS ΔWeff dependance on steam oxidation temperature. NOE PBL and TSE PBL.

4. GATE OXIDE DEFECT DENSITY

Increasing the field oxidation temperature will reduce the lateral field oxide growth induced stress in pad oxide: also, the large area (figure 4) and perimeter (figure 5) defect density of 7 nm gate oxide are improved by the field oxidation temperature increase up to 1100°C. The defect density is degraded on small geometries at low temperature and related to microtrenching(figure 2a)[4]. Substrate dependance is observed due to oxygen induced surface microroughness in Czochralski grown materials at low fields[5] and series resistance at high fields(Table1). The 1140°C large perimeter defect density degradation(figure 5) is due to the thermal expansion of oxide during the diffusion of oxygen at the recrystallized poly grain boundaries (figure 2c). The TSE PBL and NOE PBL differences are due to low temperature bird's beak growth in pad oxide (Table2). Accumulation Qbd follows the same trend reaching values of Qbd50%=10 and Qbd10%=5C/cm^2 (1100°C)

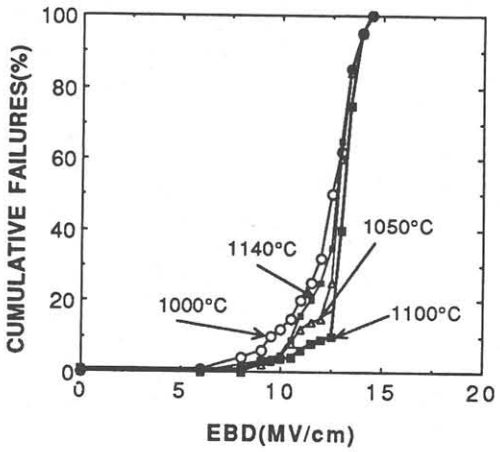


Figure 4 Active area: 17mm^2

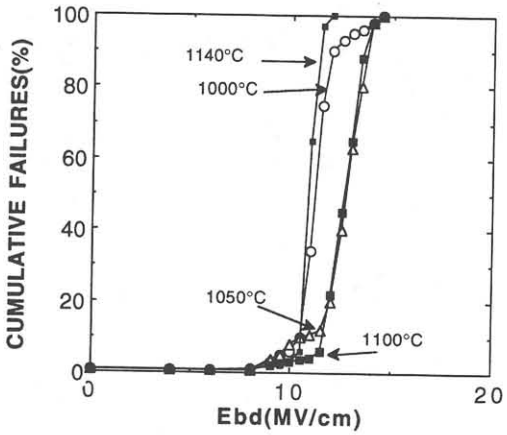


Figure 5 Active perimeter: 12m

Figures 4 & 5 HTPBL 7nm gate oxide cumulative failure as a function of breakdown field for different field oxidation temperatures. (Example of NOE PBL). Epi thickness: 4μm.

Field temperature(°C)	1000	1050	1100	1140
Material Gate ox.thk				
Epi 7 nm	0.020	0.007	0.002	0.050
Epi 12 nm	2.890	0.910	0.450	5.000
Czochralski 7 nm		0.026	0.030	0.010
Czochralski 12 nm	12.200	0.174	0.124	0.230

Table1 11MV/cm NOE PBL perimeter defectivity(def/m)

Field temperature(°C)	1000	1050	1100	1140
Etch scenario				
NOE PBL	1.480	0.200	0.180	0.200
TSE PBL	25.000	0.495	0.414	0.276

Table2 8MV/cm 12 nm gate oxide perimeter defectivity (def/m). Czochralski material.

5.ACTIVE DEVICES. IN-WELL ISOLATION.

PMOS devices were optimized using a POCl3 doped n+ polysilicon gate and a counter doped buried channel[6]. NMOS devices have been adjusted by

adding the contributions of field implant and nearly retrograde VT adjust. No narrow channel threshold voltage Vt shift is obtained on 0.25µm wide NMOS due to an appropriate channel and field doping engineering whatever the etching scenario(figure 6a). P type devices, will be more sensitive to Phosphorous sidewall pile up in the TSE PBL case (figure 6b). Gate Induced Drain Leakage(GIDL) limits drain breakdown at 10V or -10V for N or P type devices: no differences are observed between the NOE or the TSE PBL cases due to the combination of channel and drain engineering optimization.

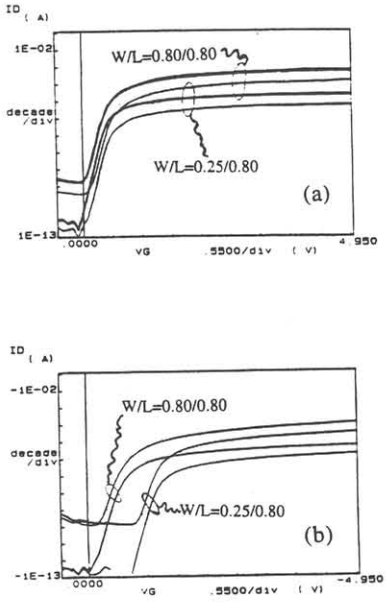


Figure 6 Subthreshold characteristics of narrow devices W=0.25µm and W=0.8µm (L=0.8µm):
(a)NMOS(Vds=0.1V;Vds=10V)
(b)PMOS(Vds=-0.1V; Vds=-10V).
TSE PBL case. Field oxidation temperature : 1100°C.

Diffusion isolation separation voltage sustaining is limited by GIDL for N and P channel poly gated devices. Instead, N metal gated devices clamping control (figure 7) is influenced by the pocketed drain avalanche resulting from the optimization of threshold implant on active transistors. Phosphorous pile up at the bird's beak edge affects the PMOS devices behaviour. The TSE PBL improves field devices clamping by the increase of field recessing. Increasing the field oxidation temperature will reduce the differences because the contribution of the sealed part of the encroachment will be more important[4].

6.ISOLATION BETWEEN WELLS.

0.6µm N-Well/n+, 0.8µm P-Well/p+ field devices clamping (worst case Vd=Vg at 10pA/µm leakage) is limited by GIDL for poly gated devices and bipolar breakdown for metal gate devices. Latch-up resistant n+/p+ distance of 2µm(1.2µm) with holding voltage of 5V(3.3V) (figure 8) is possible if 1100°C TSE PBL field isolation is combined with the use of 4µm thin p/p+ epi. Latch-up resistance improvement is

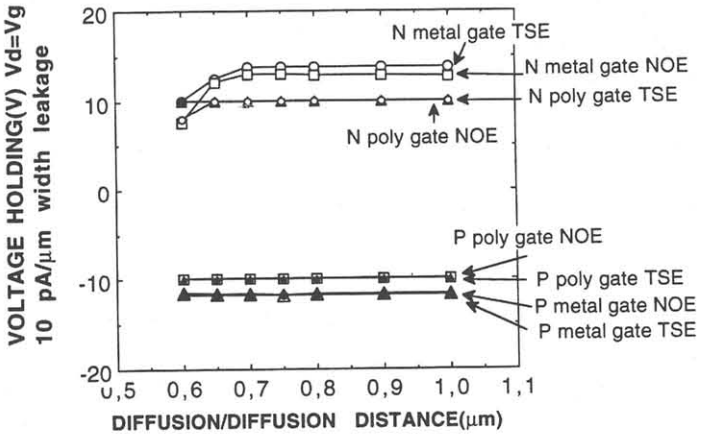


Figure 7 Poly and metal gate field transistors clamping as a function of diffusion separation distance. Field oxidation at 1100°C.

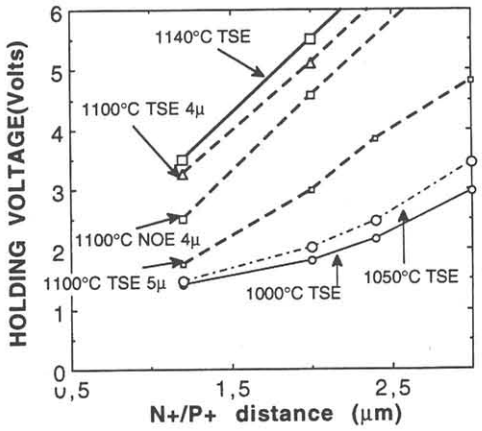


Figure 8 Holding voltage for n+/P-Well/N-Well/P+ structures as a function of n+/p+ distance for different field oxidation temperatures, etch scenario and epi thickness .

observed with increasing temperature(figure 8) due to substrate resistance decrease by higher Boron up diffusion. Steam Oxidation Enhanced Boron up diffusion will be more important in the TSE PBL than in the NOE PBL case because of the extra interstitials generated at the substrate surface during the field oxidation process resulting in a better latch-up resistance(figure8).

7. REFERENCES

[1] J.-W. Lutze et al., J. Electrochem. Soc.,Vol. 137, pp.1867-1870, June 1990
[2] S.Deleonibus and S.S.Kim 1993 SSDM Conference Tech Digest pp.525-527, Chiba, Aug.1993
[3] B.Coulmann et al. ECS Spring Meeting, Vol.89-1, Abs. n° 199, pp.293,294 May 7-12 ,1989
[4] S.Deleonibus ECS Spring Meeting 1994, Abs.n°175, pp273,274 San Francisco May 22-27, 1994
[5] S.Deleonibus et al. To be published JECS Oct. 1994
[6] G.Guégan et al. IEDM'91 Digest pp.105-108 Washington (D.C.) Dec. 1991.

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