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Highly Reliable Antifuse with TiSix/p-SiN/TiN Structure for 3.3 V Operated High Speed FPGA Application

Yoshimitsu Tamura, Hiroshi Shinriki and Tomohiro Ohta

LSI Research Laboratory, Kawasaki Steel Corp.
1,Kawasaki-cho, Chuoh-ku, Chiba 260, Japan
TEL:043-262-2468 FAX:043-262-2619

A novel antifuse with TiSix/10 nm-thick p-SiN/TiN structure has been developed for 3.3 V operated high speed FPGAs application. Lower programing voltage less than 9 V was realized by using 10-nm thick SiN film. ON-resistance of the antifuse with TiSix or TiN bottom electrode was remarkably reduced down to below 15 ohm, which is corresponding to less than 1/10 of ON-resistance obtained by conventional antifuses with n+Si/ONO/poly-Si(PLICE). However, insulative properties of 10 nm-thick SiN film formed on TiN layer were degraded greatly due to its large surface microroughness. On the other hand, the surface microroughness of the TiSix layer is greatly reduced by the reduction of formation temperature down to 650 °C and the wet chemical pre-cleaning with NH_4OH/H_2O_2 solution (APM clean). By using these processes, lifetime to breakdown of antifuses using the TiSix bottom electrode become 5 decades longer than that of antifuses with TiN bottom electrode. In addition, our proposed antifuse can be easily fabricated by adding Ti-silicidation and APM cleaning processes to the fabrication process of the conventional antifuse(PLICE). Therefore, low programing voltage, remarkably low ON-resistance are realized by this newly developed antifuse while keeping sufficient insulative property and compatibility with the conventional antifuse.

1.Introduction

The field programmable gate array (FPGA) has become an essential device for rapid implementation of digital systems. Antifuses are one of the most promising programmable elements for programmable interconnects used in FPGAs(1). Antifuses play a role as electronic switches that are normally open (off-state) and can be switched to a conducting state (on-state) only once by breaking down the insulator. Conventional antifuses (PLICE) are constructed of an insulator(ONO) between Si substrate and poly-Si as shown in Figure.1(a)(2). Recently, antifuse constructed of an insulator between metal electrodes become promising for high speed and high density FPGAs because of their low ON-resistance(3,4). The barrier metals such as TiN, TiW are used as electrodes. And as an insulator layer, NON(5) and amorphous-Si(4) are used. Lowest ON-resistance, approximately 6 ohm, is reported to be obtained by using TiN/SiNx(20 nm)/TiN structure(3). After breaking down the SiNx film, a metallic filament is thought to be formed in the SiNx film, leading to low ON-resistance. Scaling down the source voltage from 5 V to 3.3 V, the programming voltage is desirable to be reduced down to approximately 6 -10V. Thus, the thickness of dielectric film must be reduced below 10 nm in case of SiNx film. The use of thin dielectric film is advantageous to low ON-resistance because of short distance between electrodes. However, it is difficult to obtain sufficient reliability (off state) of such an extremely thin dielectric film formed on the metallic electrode such as barrier metals (TiN,TiW) due to local electric field intensification caused by the roughness of metal surface, especially sharp protrusions.

This paper describes a remarkable improvement in off-state reliability (insulative properties of 10nm-thick SiNx film) and on-state properties (ON-resistance and its distribution) by using metallic TiSix bottom electrode taking place of the TiN layer (low reliability) and N+Si (high ON-resistance). It is because that the surface microroughness of the TiSix layer is greatly reduced by the reduction of formation temperature down to 650 °C and the wet chemical pre-cleaning with NH_4OH/H_2O_2 solution (APM clean). Thus, by using this structure and these processes, highly reliable and high-performance antifuse compatible with conventional PLICE antifuse is successfully fabricated.

2.Experimental

Fabrication process flows of antifuses having TiSix/p-SiNx/TiN and TiN/p-SiNx/TiN structures and conventional antifuses are shown in Fig.1. The TiSix layer was formed by thermal reaction between Ti film(40nm) and Si substrate(RTN process), followed by the removing the residue of Ti film with H_2SO_4/H_2O_2 solution. The TiN layer was formed by reactive sputter deposition. After the surface of the bottom electrode were treated by NH_4OH/H_2O_2 solution at 70°C, the 10nm-thick SiNx film was deposited with plasma enhanced CVD method on TiSix and TiN electrodes (350°C, 0.35 torr, N_2:SiH_4:NH_3=17:5:3). The standard deviation of SiNx thickness was controlled within 2% on 6-inch wafers. The diameter of contact hole used for antifuses varies from 0.6 to 2.0 μm. Dependence of initial failure rate, I-V characteristic, dielectric breakdown voltage, TDDB and ON-resistance on process of bottom electrodes formation were measured. Antifuses were programmed with current-constant pulse (5.2msec,20mA) limited up to 12V.

And the surface microroughness of bottom electrodes before and after the APM cleaning were evaluated using Atomic Force Microscopy (AFM). The surface of TiSix film and its depth profiles were identified by Auger Electron Spectroscopy (AES).

3.Results and Discussion

We have investigated the influence of the film thickness of p-SiN and APM cleaning on the initial failure rate of antifuses using TiSix layer as bottom electrodes (Fig.2). The initial failure rate of 200 μm hole antifuse increases rapidly as the thickness of p-SiN become thinner below 20 nm. At 10 nm thickness, about 50% of antifuse are failures. It shows that it is hard to form such a thin film on the coarse metallic film surface. However, the initial failure rate is dramatically reduced by pre-treatment with NH4OH/H2O2 solution. By performing the pre-treatment, the deviation of breakdown voltage and the device area dependence of breakdown voltage on antifuses using TiSix bottom electrode became extremely smaller, however, those in antifuses using TiN bottom layer were still large (Fig.3). AFM photographs show that the pre-treatment provided smoother surface of TiSix without sharp protrusion(Fig.4). AES depth profiles of pre-treated TiSix layer shows that the coarse thin TiOxNy layer formed on the TiSix was removed and about 1.5 nm-thick SiO2 film was formed on the

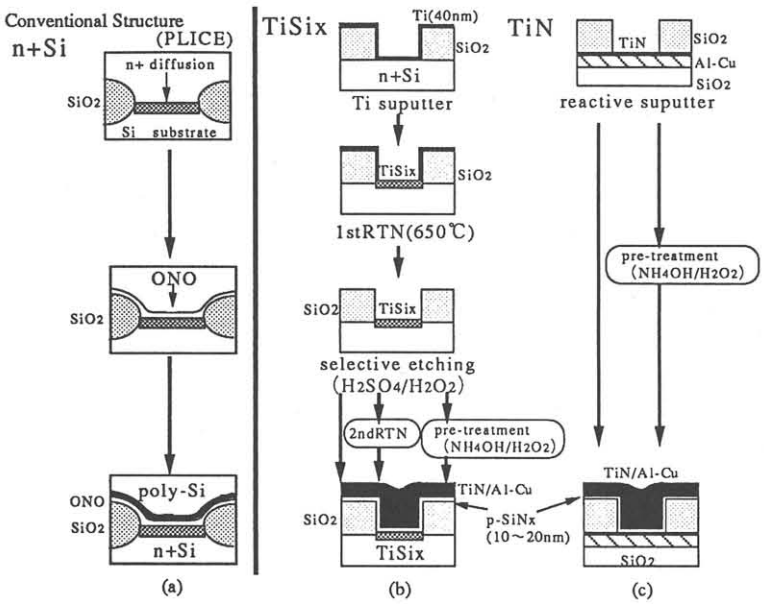

Fig.1 Schematic cross sections of Antifuse process flows

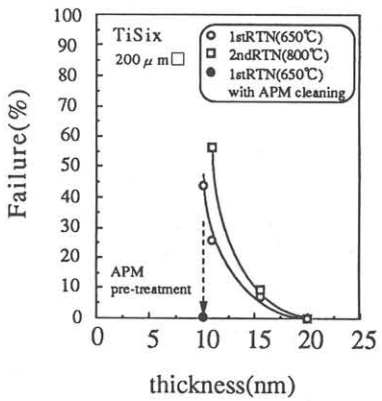

Fig.2 Percentage of initial failure versus thickness of SiN film dependent on processes

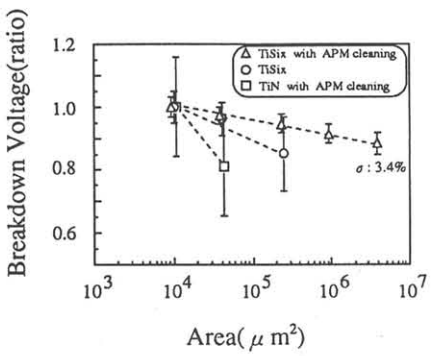

Fig.3 Breakdown voltage(ratio) versus device area compared to different processes

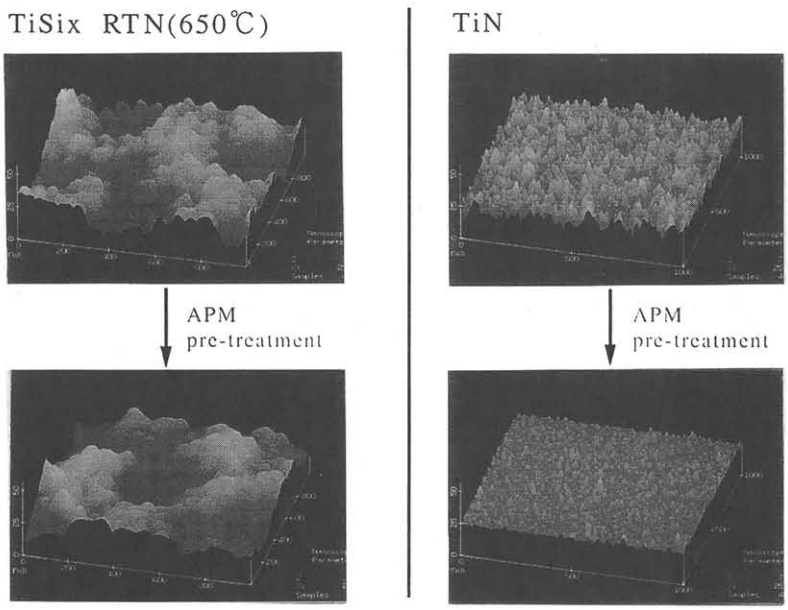

Fig.4 AFM photographes of TiSix and TiN surfaces before and after APM pre-treatment

surface of TiSix film during the pre-treatment (Fig.5). The effects of pre-treatment is thought to remove the coarse thin film on the surface and to smooth the surface of TiSix layer. It is noted here that the average surface roughness(Ra) on the TiN layer surface decreased from 2.9 nm to 0.7 nm after the pre-treatment, but that the sharpness of each protrusion seems to be still same even after the pre-treatment as shown in AFM photograph. TDDB characteristics shows that time to break down of the antifuses using TiSix electrode is estimated to be five decades longer than those using TiN electrode under 3.3 V stress voltage (Fig.6). Average ON-resistance obtained by antifuses using TiSix electrode treated with APM is 11 ohm which is less than 1/10 of ON-resistance obtained by conventional one (about 150 ohm). The ON-resistance distribution of antifuses using TiSix electrode treated with APM is much tighter than that of antifuses using TiN electrode treated with APM (Fig.7). Therefore, these

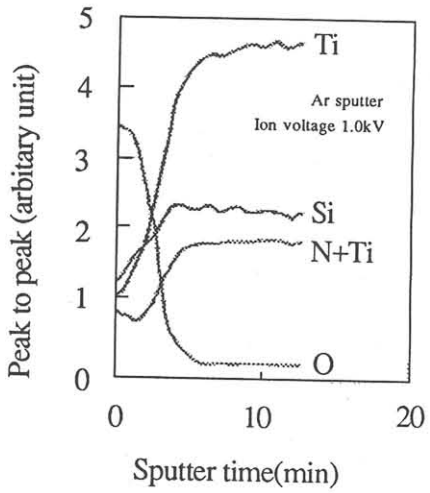

Fig.5 AES depth profiles of TiSix after APM pre-treatment

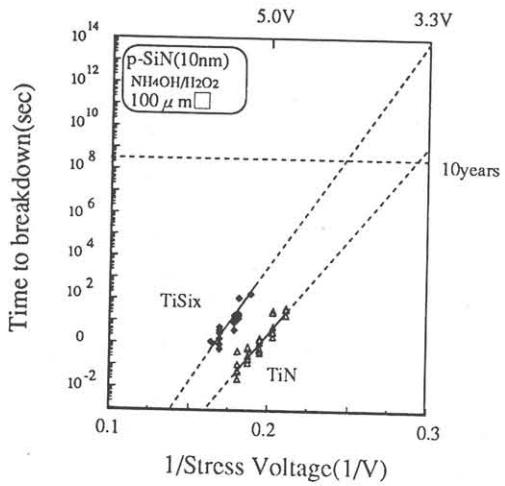

Fig.6 Comparision of TDDB characteristics of SiN(10nm) film between on TiSix electrode and on TiN electrode

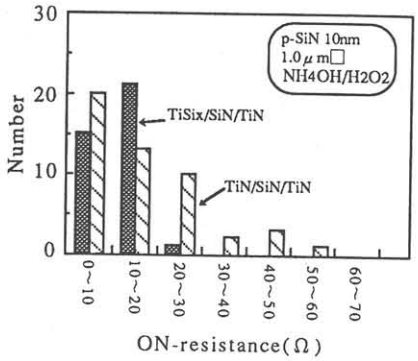

Fig.7 Histogram of ON-resistance compared between TiSix and TiN bottom electrode with APM pre-treatment

improvements in TDDB and ON-resistance are attributed to microscopically smoother surface of the TiSix layer without sharp protrusion.

4.Conclusion

Highly reliable and high performance antifuses are demonstrated to be formed by using TiSix bottom electrode without sharp protrusion and 10nm-thick SiNx film. Remarkable improvements of insulative properties and tighter distribution of ON-resistance are due to reduction of surface microroughness of the TiSix layer which is realized by reducing TiSix formation temperature down to 650°C and pre-treatment with APM solution before the deposition of SiNx film. Therefore, our developed TiSix/p-SiNx/TiN structure antifuse compatible with conventional antifuse is promising for highly reliable and very high speed FPGAs.

Acknowledgements

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