Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 473–475

Transport Properties in High Mobility Poly-Si TFTs

Tadashi Serikawa, Seiiti Shirai, Kazuo Nakagawa*), Sadao Takaoka*), Kenichi Oto*),
Kazuo Murase*) and Shuichi Ishida**)

NTT Interdisciplinary Research Labs., Musashino, Tokyo 180, Japan
*) Faculty of Science, Osaka University, Toyonaka, Osaka 560, Japan
**) Science University of Tokyo, Yamaguchi College, Onoda, Yamaguchi 756, Japan

Transport properties of high-mobility poly-Si TFTs are measured in order to clarify the role of band tail states in the grain boundaries. The poly-Si TFT with smaller carrier trap state density ($N_{st} \approx 6\times10^{11}$ cm^{-2}) in the grain boundaies show metallic behavior where the mobility increases with temperature decreasing. The poly-Si TFT with larger N_{st}($\approx 1.5\times10^{12}$ cm^{-2}) shows semiconducting behavior of mobility decreasing with temperature. At low temperature, we find on the former poly-Si TFT the resistance change due to the weak-localization effect and on the latter one Mott variable-range hopping (VRH) in the regime of strong localization. Furthermore, the Hall effect measurements show that carrier density remains essentially constant, which indicates that carrier velocity plays a more important role rather than carrier density in the transport properties even for different conduction mechanisms of poly-Si TFTs including weak-localization and Mott VRH regimes.

1. Introduction

Poly-Si TFTs are very important for new devices, such as flat-panel displays. Various approaches to fabricating high mobility poly-Si TFTs have been attempted, resulting in developing of high mobility poly-Si TFTs , especially those made from laser-annealed poly-Si films.1) Despite that there have been many investigations on poly-Si TFTs, the conduction mechanism still remains ambiguous, because of the very complex structure with grain boundaries including carrier trap states. In previous papers, 2,3) we reported that the electrical conduction at low temperatures is dominated by localized electrons in the band tail states in the grain boundaries even in a so-called high mobility poly-Si TFT. In this contribution, we further point out that poly-Si TFTs show very different features at low temperatures according to whether the sheet resistance falls below or above the characteristic resistance, $\pi\hbar/e^2$ (≈ 13kΩ) for the disorder-induced metal-semionductor (M-S) transition in two dimension (2D).4)

2. Experimental

Coplanar-structure and N-channel poly-SiTFTs were fabricated from laser-irradiated sputtered Si films and sputtered gate oxide films.5) Those mobilities at room temperature ranging from 100 to 380 cm^2/V·s have been changed by controlling laser power.6 The poly-Si TFTs have Hall-bar type electrodes in addition to gate, source and drain electrodes.2) Channel length is 110 μm and width 20 μm. In this study, we measured electrical properties, including Hall effects, of two samples A and B at temperatures between 300 K and 1.5 K. The (field-effect) mobilities for samples A and B are 260 and 150 cm^2/V·s at room temperature and carrier trap state densities N_{st} are 6×10^{11} and 1.5×10^{12} cm^{-2}, respectively. The Hall mobility which corresponds to the carrier velocity, and the carrier density were also calculated from the Hall coefficient and the conductivity.

3. Results and Discussion

Figure. 1 shows temperature dependences of sheet resistance R as parameter of gate voltage for samples A and B. Sheet resistance R in sample A decreases with temperature decreasing down to 20 K and shows metallic behavior. On the other hand, sample B shows drastic increasing of R with temperature decreasing for all gate voltages showing semiconducting behavior. Above results suggest that the border between metallic and semiconducting regimes lie near R $\approx$10kΩ.

Figures 2 (a) and (b) show temperature dependences of (Hall) mobility for samples A and B. Fig.2(a) for sample A shows increase of mobility with temperature decreasing from room temperature, and especially at high gate voltage of 30 V, it reaches 440 cm^2/V·s near 20K. The increasing indicates that phonon scattering at poly-Si/SiO$_2$ interface plays a dominant role on electrical properties. On the other hand, mobilities for sample B decrease with temperature decreasing. This is due to high potential barrier formed at grain boundaries. However, surprisingly, the carrier density is nearly independent of temperature in very wide temperature range for all gate voltages, as shown in insets in Fig.2, even in the range where sheet resistance is thermally activated. Therefore, electrical properties of poly-Si TFTs are mainly determined by the carrier velocity rather than by carrier density in the very wide temperature range even for poly-Si TFTs with different conduction mechanisms.

Two-dimensional films in the regime where sheet resistance is order of a few hundred ohms show the conductance corrections arising from the weak localization.[4)] This leads to logarithmic temperature dependence of the conductance in two dimension. As disorder becomes stronger and the sheet resistance increases , so the electron wave function is expected to exhibit strong localization in which the envelope of the wave function decays exponentially in space. A characteristics resistance for this transition is $\pi\hbar/e^2$ ($\approx$13kΩ) (roughly corresponding to N_{st}: 1.0×10^{12} cm^{-2} in our poly-Si TFTs). In the strongly-localized regime, the conductance is expected to be determined by a hopping mechanism, such as variable-range hopping (VRH) process near the Fermi level.

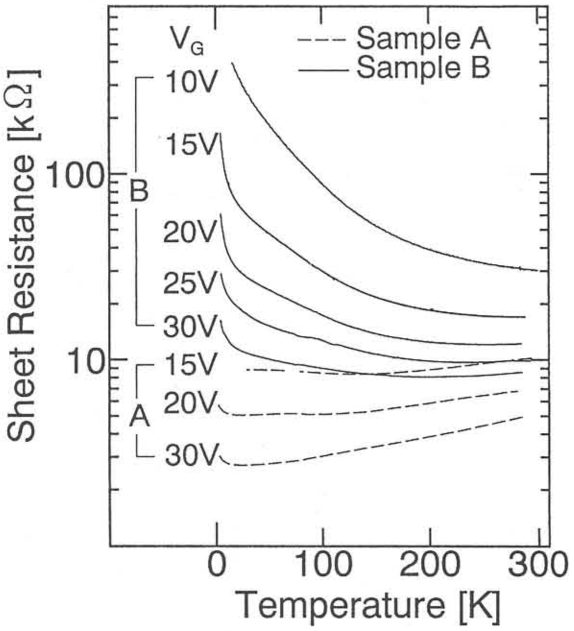

Fig.1: Dependence of sheet resistance on temperature for sample A and sample B.

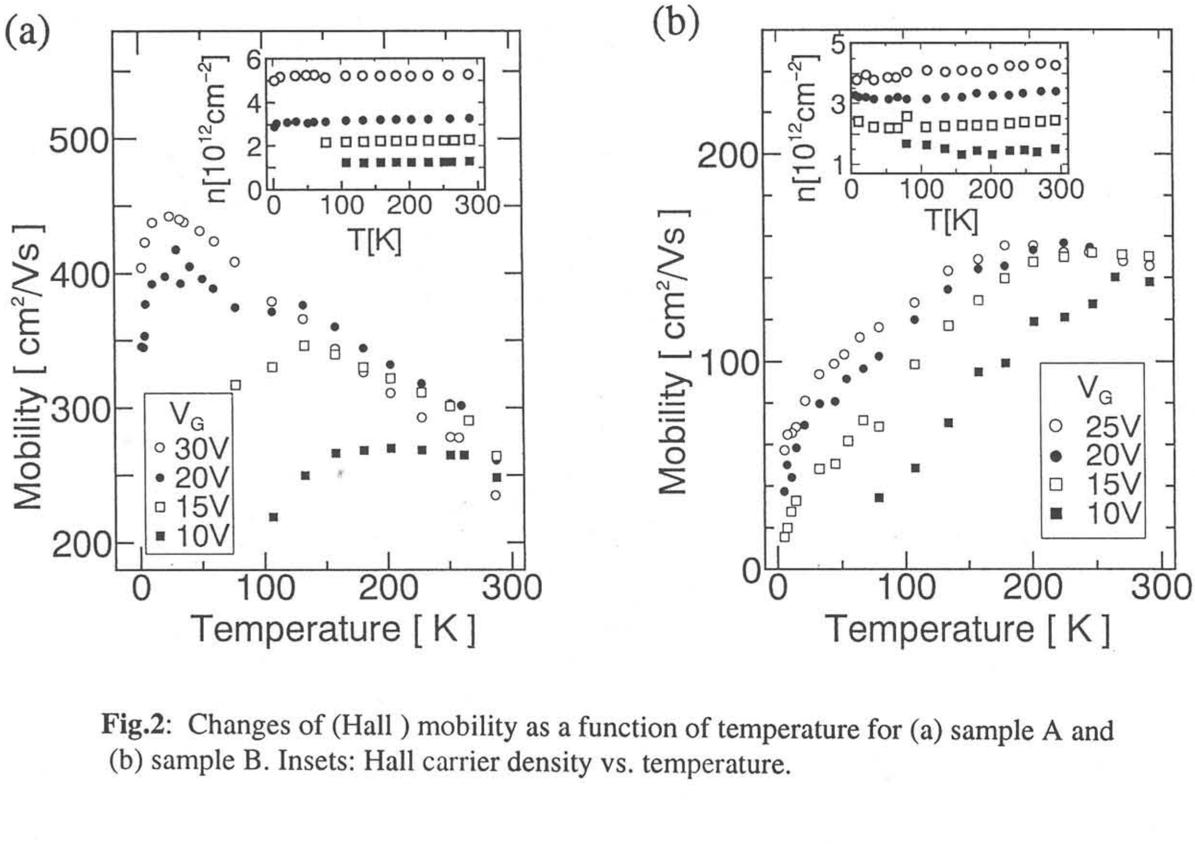

Fig.2: Changes of (Hall) mobility as a function of temperature for (a) sample A and (b) sample B. Insets: Hall carrier density vs. temperature.

Figure 3 shows plots of sheet conductance vs. logarithmic temperature for sample A at gate voltages of 20 V and 30 V. Below 10K, sheet conductance obeys the logarithmic temperature dependence due to the weak localization of states in the grain boundaries.[6] At these temperatures, negative magnetoresistance (MR) was observed, and satisfactorily fitted to the prediction by weak-localization theory.[4] Figure 4 shows the sheet resistance vs. cube root of temperature for sample B. Below about 40K, the resistance R obeys $R=R_0\exp((T_0/T)^{1/3})$ law arising from 2D VRH between strongly-localized states.[7] For sample B also, the negative MR was observed at these temperatures.

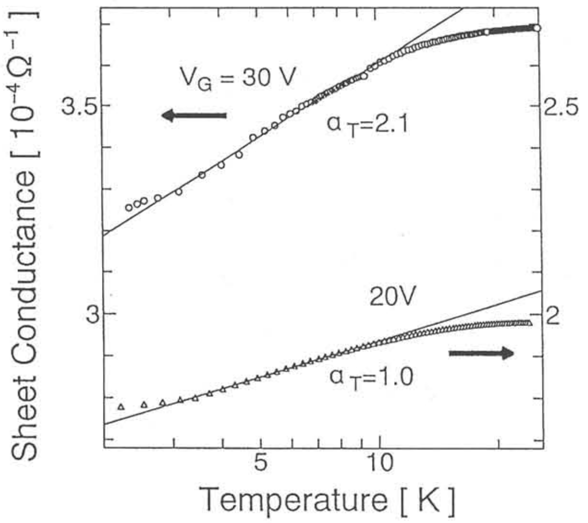

Fig.3: Sheet conductance - ln(T) plots in poly-Si TFT (Sample A) at gate voltages of 20V and 30V.

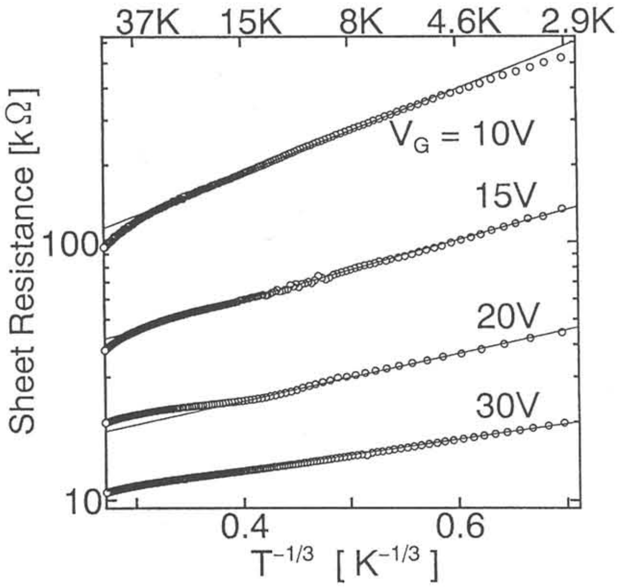

Fig.4: Temperature dependences of sheet resistance in poly-Si TFT (Sample B) at various gate voltages.

It arises from quantum interference of different hopping paths between two localized states. [3]

The above weakly- and strongly- localized behaviors of electrons are explained by the mobility edge model. However, the Hall effect does not probe extended states from our results. This problem seems to be the same as that observed in crystalline Si MOS in the barely-insulating regime near the metal-semiconductor transition.[8]

4. Conclusion

Electrical properties of poly-Si TFTs with different carrier trap state densities N_{st} were measured in the wide range of temperature. It was newly found that poly-Si TFTs show different conduction mechanisms for slight change of the carrier trap state density. The poly-Si TFT with smaller N_{st} shows metallic behavior and the mobility increases with temperature decreasing. On the other hand, the poly-Si TFT with larger N_{st} shows semiconducting behavior where the mobility decreases with temperature decreasing. At low temperatures, poly-Si TFT with smaller N_{st} shows the weak localization effect and the one with large N_{st} shows Mott variable-range hopping (VRH). Futhermore, Hall effect measurements show that carrier velocity plays a more important role rather than carrier density in the transport properties even for the poly-Si TFTs with different conduction mechanisms.

Acknowledgments

The authors would like to thank A. Okamoto and S. Suyama for helping with poly-Si TFT fabrication, and A. Kudoh and Y. Tsutsui for measuring the electrical properties of the poly-Si TFTs.

References

1) for example, K. Shimizu et al., IEEE Trans. Electron Devices, 40(1993) 112.
2) T. Serikawa, et al., Jpn. J. Appl.Phys., 33 (1994) L.409.
3) S. Ishida, et al., J. Phys. Soc. Jpn. 63 (1994) 1254.
4) P. A. Lee and T. V. Ramakrishnan, Rev. Mod. Phys., 57 (1985) 287.
5) T. Serikawa, et al., IEEE Trans. Electron Devices, 36 (1989) 1929.
6) S. Shirai, et al., IEEE Trans. Electron Devices, 39 (1992) 450.
7) N. F. Mott, J.Non-Cryst. Solid, 1 (1968) 1.
8) E. Arnold, Surf. Sci., 58 (1976) 60.