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Application of As-Deposited Poly-Crystalline Silicon Films to Low Temperature CMOS Thin Film Transistors

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As-deposited poly-crystalline silicon (poly-Si) films have been applied to low temperature processed complementary metal oxide semiconductor (CMOS) thin film transistors (TFTs). Continuous two-step deposition of poly-Si films in the infra-low pressure chemical vapor deposition (ILPCVD) reduces the maximum processing temperature through the CMOS TFT fabrication to 555° C and eliminates the troublesome need for crystallizing silicon films. CMOS static shift registers have been successfully integrated on a glass substrate.

INTRODUCTION

Low temperature processed poly-crystalline silicon (poly-Si) thin film transistors (TFTs) have demonstrated a wonderful ability to compose the integration of CMOS circuits on conventional glass substrates[1]. They have also shown remarkable possibilities for production of large-area[2] and high-quality liquid crystal displays (LCDs) with integrated drivers[3]. All the low temperature processed poly-Si CMOS TFTs so far have utilized crystallization of silicon films either by irradiation of laser beams[3,4,5] or by thermal annealing in a furnace[6]. These technologies can definitely improve transistor characteristics. They are, however, still far from practical use in industry mainly because it is difficult to obtain uniformity with laser irradiation and because the severe temperature conditions attending furnace annealing cause glass deformation. Rather than treating these crystallization technologies, this paper deals with simple as-deposited poly-Si films by the low pressure chemical vapour deposition (LPCVD) using silane (SiH_4) as a raw material and their application to low temperature processed CMOS TFTs. The maximum processing temperature is reduced to 555° C without relying on any crystallization.

PREPARATION OF POLY-Si FILMS BY TWO-STEP DEPOSITION

The ILPCVD[7] has prepared high quality as-deposited poly-Si films at 555° C, using mono-silane (SiH_4) as a raw material. It is well known that low silane partial pressure (P_{SiH4}) in an LPCVD reactor is preferable to high pressure both for high quality as-deposited poly-Si films and, consequently, for TFTs at a fixed temperature[8,9,10]. However, the very low pressures such as 0.15 mtorr at 555° C hardly form any silicon films with the conventional one-step deposition. This is due to very long incubation time for the deposition; in other words, to a very slow nucleation rate in the early film formation. The deposition process of poly-Si films consists of the initial silicon nucleation on the SiO_2 surface and the following growth of the silicon nuclei[11]. It is the very slow nucleation rate that prevents the deposition. Therefore, we have adopted continuous two-step deposition, which enables us to obtain good poly-Si films at 555° C. The two-step deposition is composed of the first deposition with the higher partial pressure of silane and the successive second one with the lower partial pressure. The first deposition accelerates the nucleation rate and forms the approximately 9.0 nm-thick bottom part of the films, while the second deposition improves film quality and forms the 18 nm-thick (at least) central and top parts of the films. Figure 1 shows the film growth rate depending on P_{SiH4} during the second deposition. The silane flow rate was fixed to 100 sccm during the first deposition for all samples, resulting in the P_{SiH4} of 0.94 mtorr. The first deposition stretches for 30 minutes. Varying the silane flow rate between 5 sccm and 70 sccm creates various values for the P_{SiH4} during the second deposition. Even 50 μ torr (0.05 mtorr) of silane partial pressure deposits poly-Si films, thanks to the continuous two-step deposition.

PHYSICAL AND ELECTRICAL PROPERTIES OF THE POLY-Si FILMS

Non-self-aligned NMOS poly-Si TFTs in a top gate structure were fabricated through low temperature process in order to evaluate the electrical characteristics of these as-deposited poly-Si films. The thickness of the channel poly-Si films is 27.5 nm. Lowering the P_{SiH4} clearly but slightly improves all electrical properties of the poly-Si films, such as mobility value, threshold voltage, on-current and off-current. The dependence of the mobility value on P_{SiH4} during the second deposition is drawn in Fig. 2 as an example. The poly-Si films at P_{SiH4} = 0.10 mtorr have the maximum mobility value of 5.5 $cm^2 \cdot v^{-1} \cdot s^{-1}$ and the minimum threshold voltage of 2.5 v. The source drain currents of transistor on-state (Vds = 4

v, Vgs = 10 v) and of transistor off-state (Vds = 4 v, Vgs = 0 v) are 2.8 μA and 0.044 pA respectively, resulting in high on/off current ratio of nearly ten to the eighth power.

Other physical analyses confirm that the best as-deposited poly-Si film is obtained at P_{SiH4} = 0.10 mtorr as well. Transmission electron microscopy (TEM) observes that the films at P_{SiH4} = 0.10 mtorr consist of larger grains (Fig. 3-a) than do those at higher pressure, e. g. P_{SiH4} = 0.70 mtorr, (Fig. 3-b). The gray background in the TEM photographs is thought to be the amorphous state, while the many black spots are thought to be crystallite. The low pressure film (Fig. 3-a) clearly has higher crystalline density than does the high pressure one (Fig. 3-b). Scanning electron microscopy (SEM) photographs also show that poly-Si films at P_{SiH4} = 0.10 mtorr are made up of the biggest grains. The films deposited at 0.05 mtorr are found to contain many voids and, therefore, are so porous that the corresponding transistors degrade the electrical properties. This phenomenon has been already reported elsewhere[12]. One of the possible causes of the void generation is the presence of some contaminant, such as oxygen or water, in the poly-Si films. Although the full details of the mechanism of the void generation are still unclear, a further increase of the pumping speed of the ILPCVD together with a further increase of the silane flow rate will certainly solve this problem and improve the as-deposited poly-Si film quality. In addition it will increase the poly-Si deposition rate.

APPLICATION TO THE CMOS CIRCUIT

960-bit CMOS static shift registers have been integrated on a glass substrate with the low temperature processed self-aligned TFTs. The best quality as-deposited poly-Si films formed at P_{SiH4} = 0.10 mtorr and T = 555° C are used as a channel layer for the CMOS TFTs. The thickness of the poly-Si is 64.8 nm. An electron cyclotron resonance plasma enhanced CVD (ECR-PECVD) prepared 122.4 nm SiO_2 films as a gate insulator. The substrate temperature during the SiO_2 formation is 100° C. A 150 nm layer of chromium (Cr) sputter-deposited at 150° C serves as a gate electrode, on which a 350 nm SiO_2 layer is formed by an atmospheric pressure CVD (APCVD) at 300° C. This layer protects the channel region from the subsequent ion implantations. Both phosphine (PH_3) and diborane (B_2H_6) diluted into hydrogen were implanted by a non-mass-separated ion-implanter for forming source and drain regions of NMOS TFTs and PMOS TFTs, respectively[13]. An interlayer SiO_2 was deposited by APCVD at 300° C. The following two-hour furnace annealing at 350° C activates implanted ions and packs the interlayer SiO_2 tightly. Both indium tin oxide (ITO) as the pixel electrode and aluminium (Al) as the interconnection were sputter-deposited at 150° C and 180° C, respectively. Therefore, the most severe heat environment through the TFT fabrication is during the poly-Si deposition. It is 5 hours at 555° C.

Figure 4 presents I_{ds}-V_{gs} characteristics of the resultant NMOS and PMOS TFTs. The mobility and threshold voltage of the NMOS TFTs are 7.8 $cm^2 \cdot v^{-1} \cdot s^{-1}$ and 5.9 v. Those of PMOS TFTs are 4.0 $cm^2 \cdot v^{-1} \cdot s^{-1}$ and -9.7 v. CMOS circuits function appropriately. The maximum clock frequency of the 960-bit CMOS shift register is drawn in Fig. 5 as a function of supply voltage. The operation speed is not very fast now, for example f_{max} = 450 kHz at V_{dd} = 17 v, though it is fast enough for a scan driver circuit of any LCD. In addition the optimization of the circuit design or of the TFT dimension can improve it further.

CONCLUSION

Continuous two-step deposition with very low silane pressure in the ILPCVD makes as-deposited poly-Si films applicable to the low temperature processed CMOS TFTs. Since this technology does not use any crystallization methods but only uses low temperature (555° C) LPCVD method, low temperature processed CMOS TFTs are liberated from the problems such as non-uniformity, glass deformation, low through-put, and area restrictions, resulting in the early application to reliable LCD fabrication.

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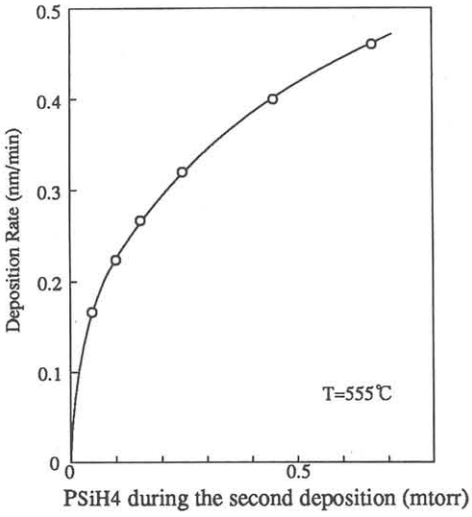


Fig.1

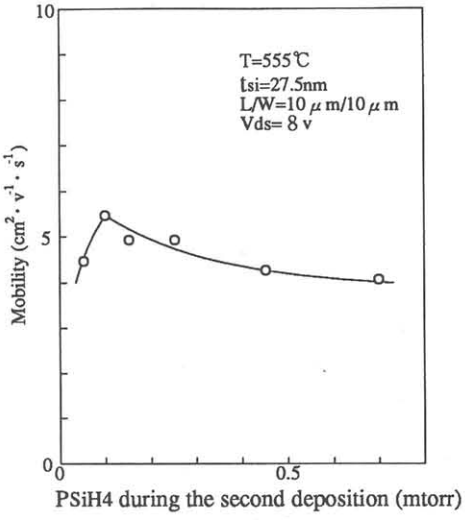
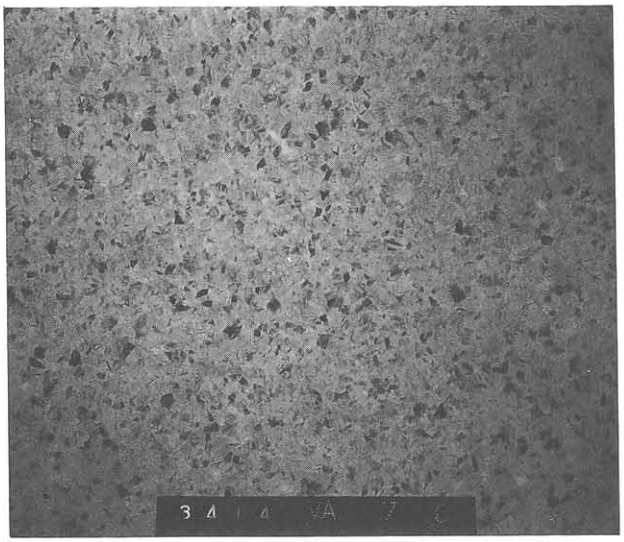
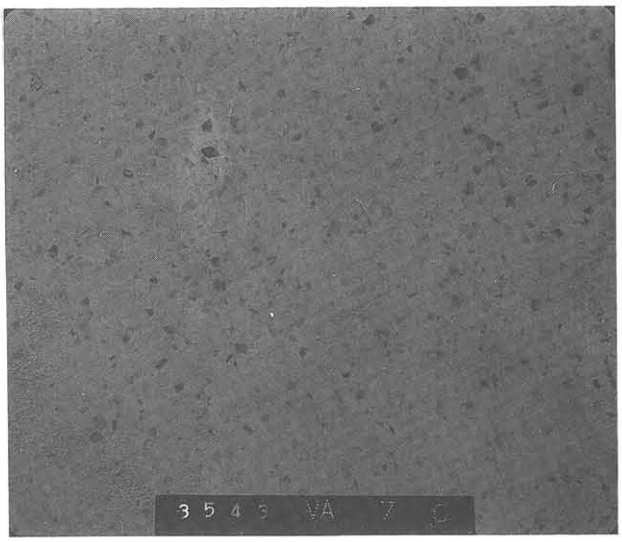


Fig.2



⊢⊣ 100nm

Fig.3-a P_{SiH_4}=0.10mtorr



⊢⊣ 100nm

Fig.3-b P_{SiH_4}=0.70mtorr

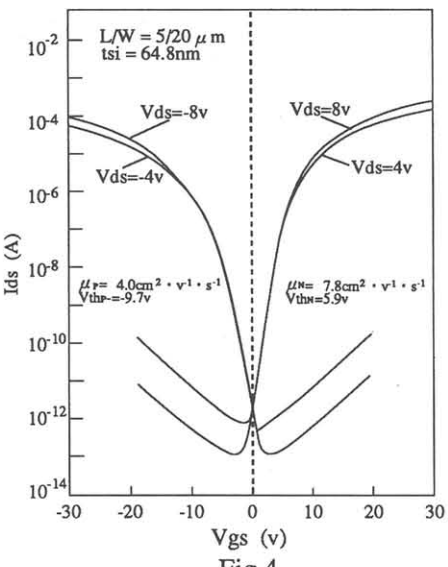


Fig.4

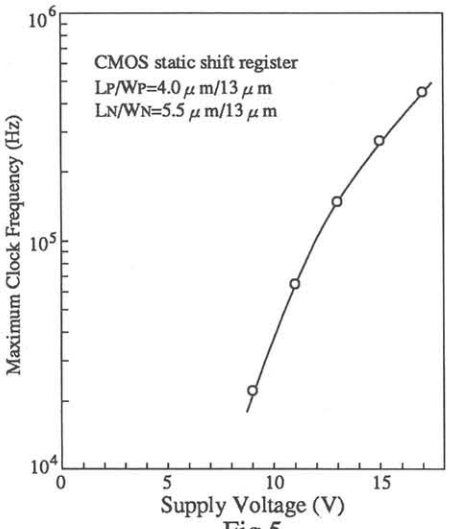


Fig.5