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Quantized Conductance of a Silicon Wire Fabricated Using SIMOX Technology

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An ultra-fine silicon wire has been fabricated using the SIMOX (Separation by IMplanted OXygen) technology, electron beam lithography, anisotropic chemical etching, and thermal oxidation. The wire exhibits quantized conductance at 26 K, while conductance plateaus remain up to 60 K. This is attributed to the large subband energy spacing in a narrow constriction successfully formed by using physical confinement with a high potential SiO_2 barrier.

1. Introduction

Recent progress in semiconductor processing technology has enabled us to fabricate submicron-size devices, and has reduced sample dimesionality. To overcome the operational limits of silicon devices, quantum phenomena, such as quantized conductance, in a quasi-one-dimensional (1D) system have been studied extensively.[1-5] Up to now, however, electron confinement has been achieved mainly by electrostatic potential, where the 1D subband energy spacings are generally limited to several meV because of the shallow potential profile formed by the fields using the gate.

In this work, we report the fabrication of a physically-confined silicon quantum wire on a SIMOX (Separation by IMplanted OXygen) wafer and present the results of conductance measurements at relatively high temperatures. SIMOX is an excellent SOI (Silicon On Insulator) fabrication technique due to its good homogeneity [6] of the thin silicon film on buried SiO_2. Vertical confinement is automatically attained by using the SOI structure. Horizontal confinement is attained by electron beam (EB) lithography, anisotropic chemical etching, and thermal oxidation, which makes it possible to fully surround silicon wires with SiO_2 having smooth boundaries.

2. Fabrication Process

The devices used in this work, shown schematically in Fig. 1(a), are n^+ polycrystalline silicon (poly-Si) gate MOSFETs with a narrow wire fabricated on an n-type (001) SIMOX wafer. The initial thickness (about 200 nm) of the top silicon layer of the SIMOX wafer was reduced to about 50 nm by thermal oxidation at 1100℃. Source and drain (S-D) areas with a <110> directional silicon wire were patterned by EB lithography (Fig.

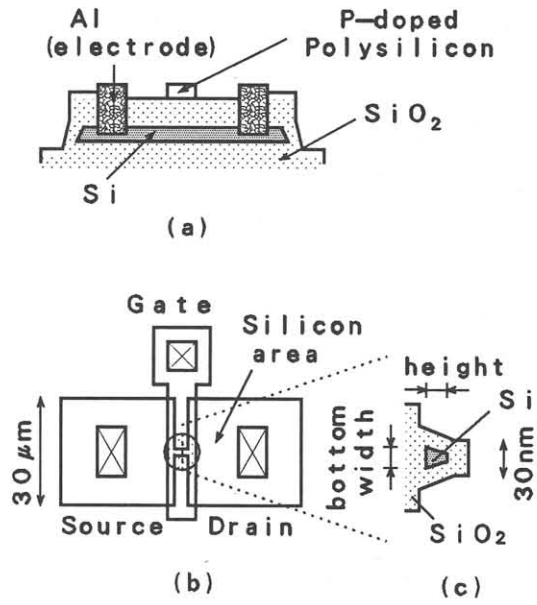


Fig.1 Schematic diagram of the device structure; (a) cross section, (b) top view, (c) expanded cross section of the silicon wire. A silicon quantum wire with a trapezoidal cross-section is formed in the center of the source and drain regions under the gate, shown by the circle in (b).

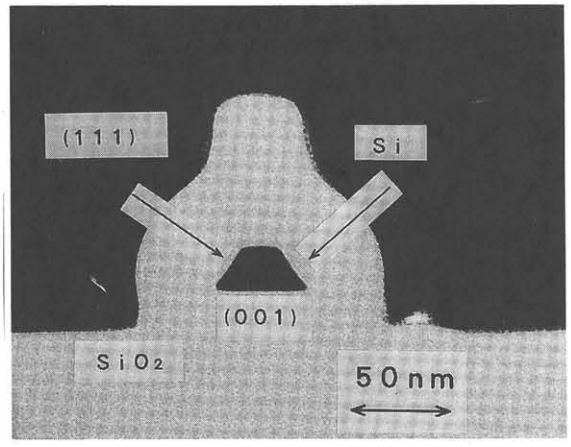


Fig. 2 Cross sectional TEM photograph of the wire.

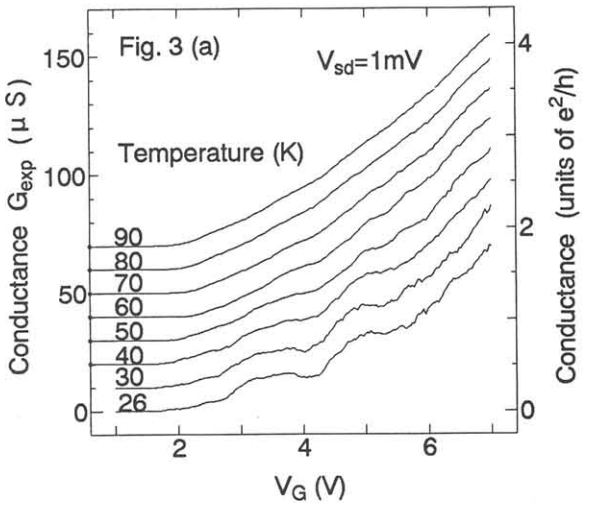
1(b)). After reactive ion etching of the SiO_2 mask layer, and anisotropic wet etching of silicon in KOH solution, the size of the wire was measured by SEM and AFM. Its minimum size was 30 nm in both width and length. Subsequent thermal oxidation at 1000 ℃ yield a narrower silicon wire with a trapezoidal cross-section surrounded by SiO_2 (Fig. 1(c)). A phosphorous-doped poly-Si gate electrode was then formed on the wire, followed by phosphorous-ion implantation into the silicon layer at the S-D regions at a doping concentration of 1×10^{21} cm^{-3} and annealing at 1000℃. The final size of the wire used for the 1D transport studies was typically 20 ± 2 nm in width, 6 ± 2 nm in height and 100 ± 10 nm in length (along the current flow), as estimated from the thermal oxidation rate.

Figure 2 shows a cross-sectional TEM photograph of a long wire fabricated by the same KOH etching and thermal oxidation process. This figure clarifies that an ultra-fine (45-nm wide, 22-nm high, and 400-μm long) wire with a trapezoidal cross-section and smooth Si/SiO2 boundary has been formed without any defects.

3. Experiments and Discussions

Two-terminal conductance was measured in a cryostat system from 25 K to 100 K. For this, the drain voltage was mainly set at 1 mV ($<< k_BT/e$ in the present temperature range).

Figure 3(a) shows the gate voltage V_g dependence of the conductance at various temperatures. Plateaus in the conductance can be seen at 26 K, and are still present at 60 K. In measuring quantized conductance, a subband energy separation of at least 3.5 k_BT is required to observe conductance plateaus.[7] From $T\approx70$ K where the steps almost disappear, we roughly estimate the spacing to be ≈20 meV for the two lowest levels in the 1D region. This is consistent with the source-drain voltage V_{sd} dependence of the conductance shown in Fig. 3(b), because the steps disappear at



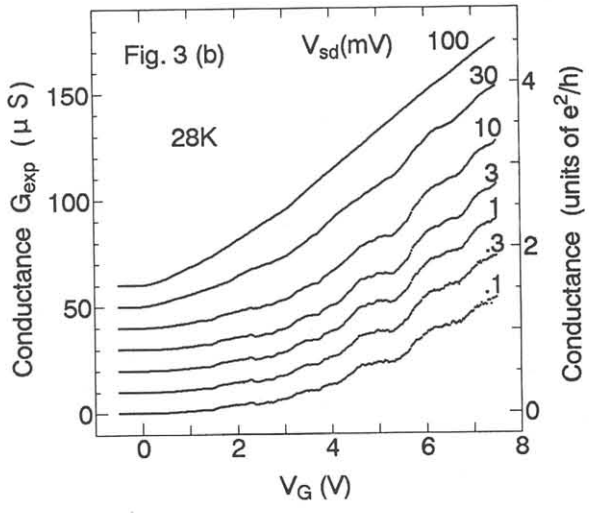


Fig. 3 Gate voltage V_g dependence of the experimental conductance at various (a) temperatures and (b) source-drain voltages. The curves are offset vertically for clarity.

100 meV, at which point voltage across the wire region is 15～20 meV. These results confirm that large energy spacing is realized in this physically-confined silicon wire.

If no backscattering occurs in the quantum wire, the wire conductance G_W is given by the Landauer formula,[8] $G_W = g_s g_v N(e^2/h)$, where g_s and g_v are the spin degeneracy and valley degeneracy, respectively, and N (integer) is the channel number. In our <110> directional silicon wire system, a steplike increase in the conductance with spacings of $4e^2/h$ ($g_s = g_v = 2$) or $8e^2/h$ ($g_s = 2$, $g_v = 4$), depending on the cross-sectional shape, is expected as the number of occupied 1D subbands increases. The quantized steps in Fig. 3, however, are about $0.6\,e^2/h$ because the parasitic series

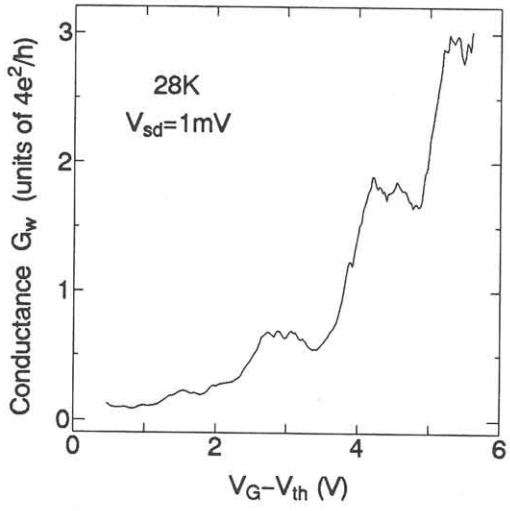


Fig. 4 The wire conductance G_w as a function of gate voltage V_g. Series resistance G_s^{-1} was subtracted.

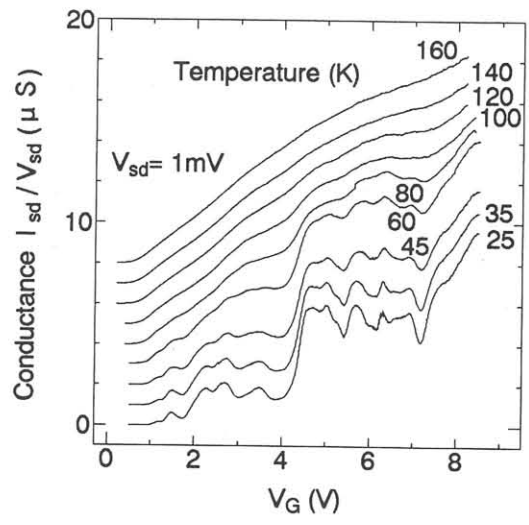


Fig. 5 Gate voltage V_g dependence of the experimental conductance of the most ultra-fine wire in this work. The curves are offset vertically for clarity.

resistance of our device significantly reduces the total conductance. The measured conductance G_{exp} is :

$$G_{exp}^{-1} = G_w^{-1} + G_s^{-1}, \quad (1)$$

where G_s is the conductance of the parasitic series resistance which is produced in S-D regions and non-phosphorus-ion-implanted silicon regions adjacent to the wire under the gate. Since the present fabrication process makes the S-D regions very thin with almost the same silicon thickness as in the wire region, large parasitic resistance and quantized resistance coexist.

To estimate G_s^{-1}, we measured the conductance of a two-dimensional (2D) silicon MOSFET without a wire fabricated on the same wafer. The conductance of the 2D MOSFET G_0 was reasonably $G_0 = \alpha(V_g - V_{th})$, for a small drain voltage. Figure 4 shows the V_g dependence of the wire conductance G_w at 28 K obtained by subtracting G_s^{-1} (= $(\alpha'(V_g - V'_{th}))^{-1}$) from G_{exp}^{-1} in Eq. (1). α' and V'_{th} of G_s^{-1} were used as fitting parameters for Eq. (1). The plateaus in the conductance at multiples of $\approx 4e^2/h$ are shown in Fig. 4. In this procedure, the fitted value of V'_{th} was about 2 V larger than V_{th}, while the fitted α' was almost the same value as α. This discrepancy between G_s and G_0 may be related to carrier trapping at the Si/SiO_2 boundary, or wide-narrow (wire)-wide structural effects on parasitic resistance. Further investigation is needed to understand the physical meaning of this necessitated V_{th} shift.

We also measured an conductance of the ultimately-fine wire (18 ± 2-nm wide, 5 ± 2-nm high and 60 ± 10-nm long), the smallest among our samples. As seen in Fig. 5, though huge parasitic resistance ($\approx 250\ k\Omega$) significantly suppresses conductance, the steplike structure remains up to ≈ 100 K.

4. Conclusion

We have fabricated a silicon wire on a SIMOX wafer. In this wire, quantized conductance steps were observed at 26 K, and remained up to 60 K, the highest temperature ever reported for silicon 1D systems. Large subband energy spacing has been realized by physical confinement with a high-potential SiO_2 barrier.

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