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Quasi-One Dimensional Conduction in Polycrystalline Silicon Nano Wire

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Electrical conduction characteristics of polycrystalline silicon (poly-Si) nano wire between temperature of 300 K and 2 K are reported. The nano wire, 5-8 nm wide, 10-20 nm high and grain length of around 100 nm is fabricated by the self-aligned confinement of a 100 nm wide and 100 nm deep trench formed in silicon substrate. The resistance increases with the reduction of temperature, which might be attributed to the weak localization phenomena due to the quasi-one dimensional structure of the nano wire. The conductance exhibits a gap of about 30 mV below 10K, which is attributed to a barrier height of about 1 meV at the grain boundary of the poly-Si layer.

1. INTRODUCTION

Quantum devices[1] are some of the most promising candidates to supersede silicon MOSFET's, which would be limited to further microminiaturization beyond the 100 nm technology level[2]. However, most activity has been focused on compound semiconductors and very few attempts have been made to fabricate silicon nano structures except for gate-controlled quantum inversion layers[3], oxidation thinned silicon columns[4] and polycrystalline silicon (poly-Si) grain wires[5]. A silicon nano wire would make it possible to fabricate high performance optoelectronic integrated circuits with light emitting silicon by using the quantum confinement effect[6], and to realize single electron tunneling devices[7]. This paper demonstrates quasi-one dimensional conduction characteristics in the polycrystalline silicon (poly-Si) nano wire[8].

2. NANO WIRE FABRICATION PROCESS

The fabrication process of the nano wire is schematically shown in Fig. 1, which consists of forming a 100 nm wide pattern by electron beam lithography, etching of a 100 nm deep trench by reactive ion etching (a), conformable filling of the trench by a low pressure chemical vapor deposition (LPCVD), slit etching (b), a 1 x 10^{20} cm^{-3} phosphorus doped LPCVD amorphous silicon (a-Si) deposition (c) and etch back (d). The resulting dimensions of the nano wire measures about 5-8 nm in width and 10-15 nm in height, measured by cross section transmission electron microscope (X-TEM[9] : Hitachi H-9000 HUR). An annealing at 1000°C for 1 hour in a dry nitrogen atmosphere crystallized the a-Si to poly-Si nano wire, with an average grain length of 100 nm, as

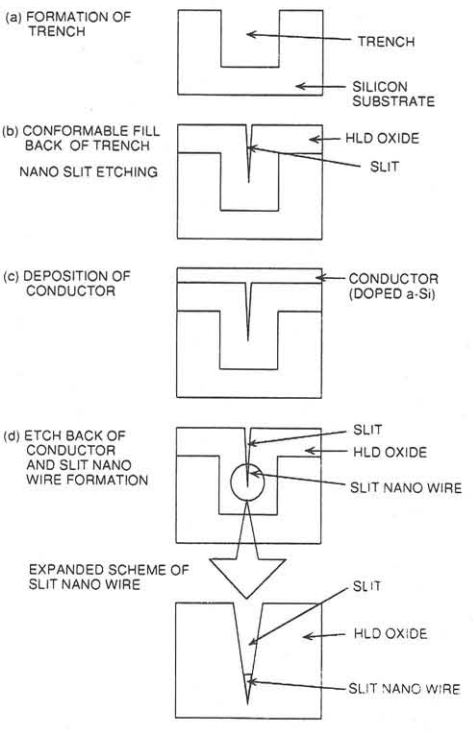

Fig. 1 Cross section of poly-Si nano wire fabrication process
(a) trench formation by lithography and etching
(b) conformable filling of trench
(c) LPCVD a-Si deposition
(d) etch back

ascertained by the plan view TEM observation depicted in Fig. 2. The device structure used in the experiment is schematically depicted in Fig. 3, which would make it possible to place electric contacts on both sides of the nano wire structures, and to design devices with suitable dimensions and arbitrary structures. The nano wire length was designed as 3 μm, and about 30 grains exist within a nano wire.

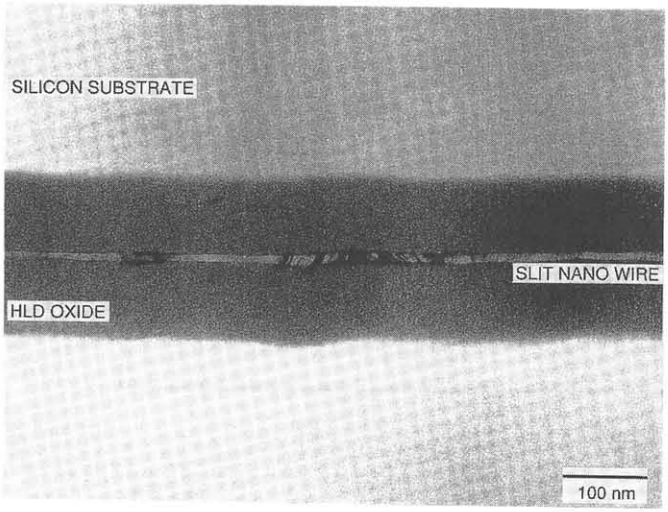

Fig. 2 Plan view TEM micrograph of the nano wire annealed at 1000°C

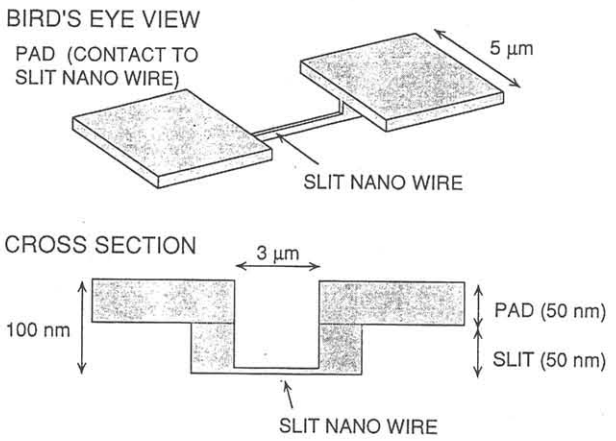

Fig. 3 Schematic drawing of the nano wire device structure

3. RESULTS AND DISCUSSION

Current-voltage (I-V) characteristics measurement was carried out between the temperature of 300 K and 2 K. The conductance lowered with the lowering of the temperature (T), as shown in Fig. 4, and revealed a gap below the temperature of about 10 K, which measured about 30 meV at 2 K. The barrier height should be about 1 meV, since the temperature at which the gap begins to appear is 10 K. Therefore, assuming that each grain boundary acts as a tunneling barrier height of 1 meV, then the total gap energy would be around 30 meV (1 meV x 30), which well corresponds to the TEM observation. These results indicate that the nano wire would show coulomb blockade phenomenon when cooled down to a low enough temperature.

Conductance characteristics shown in Fig. 5 are contrary to the observations on flat poly-Si layers with more than a 3.5 x 10^{19} cm^{-3} phosphorus doped layers, which indicates metallic conduction[10]. The I-V characteristics shown in Fig. 4 were analyzed based on the weak localizing model, and r vs. ln T plot indicates almost linear relationship, as shown in Fig. 6. In the figure, the conductance data are also plotted during cooling and warming between temperatures of 300 K and 10 K. The discrepancy between those data may be caused by the non-equilibrium measurement during cooling and warming. Thus, the decease of conductance of the nano wire at lower temperatures can be attributed to the weak localization of carriers due to the quasi-one dimensional conduction effect in less than a 10 nm diameter wire[11].

Single crystal silicon nano wire structure would be desirable for optoelectronic device applications. Experimental results indicate that the grains grew to a size of more than about 2 μm for samples annealed at 540°C for over 100 hours[12]. Thus optoelectronic LSI should be made possible by fabricating nano wires on CMOS and/or bipolar LSI's with compatible processing technologies. On the other hand, smaller grain size would be preferable for single electron tunneling (SET) devices, since the operation characteristics depend on the capacitance of the quantum dot[7]. This would be achieved by choosing high temperature, short time annealing conditions[12].

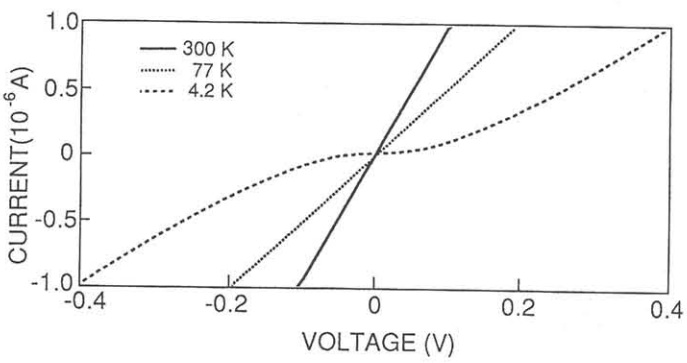

Fig. 4 Current -voltage characteristics of the nano wire at 300 K, 77 K and 4.2 K ; a 30 mV gap appears at 4.2 K

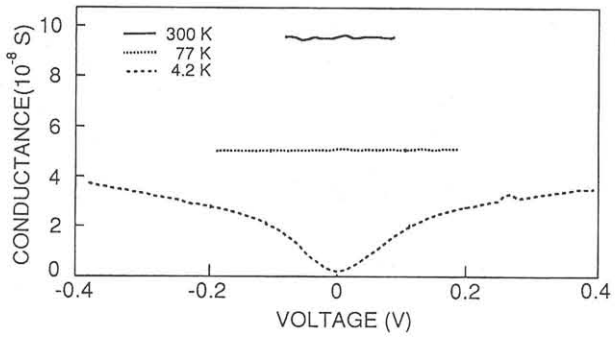

Fig. 5 Conductance of the nano wire at 300 K, 77 K and 4.2 K

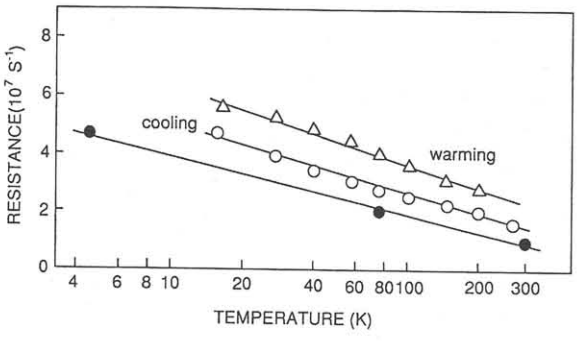

Fig. 6 Conductance analysis based on the weak localization model
solid circle :derived from Fig. 4,
open marks :data taken between 300 K and 10 K

4. CONCLUSION

This paper reported electrical conduction characteristics of polycrystalline silicon (poly-Si) nano wire between room temperature and 2K, with width and height of less than 10 nm and grain length of around 100 nm. The resistance increased with the reduction of temperature, which might be due to the weak localization of carriers in the quasi-one dimensional structure of the nano wire. The conductance exhibits dip below 10K, which was attributed to a 1 meV barrier effect of the grain boundary of the poly-Si layer.

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