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# A Consistent Model for Polarity Dependence of Threshold Voltage Shift in Fowler-Nordheim Stressed CMOS Transistors

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The paper discusses the threshold voltage degradation of CMOS devices due to high field oxide stressing. It is shown, that monitoring of stress voltage transients during constant-current electron injection into the device gate oxide may be very helpful in understanding degradation phenomena. A qualitative model is proposed to explain different behavior and susceptibility of the threshold voltage of CMOS devices to F-N stress-induced degradation. The model is based on differences in charge trapping and detrapping in different regions of very thin gate oxides under different stress conditions in PMOS and NMOS transistors.

## 1. INTRODUCTION

The Fowler-Nordheim (F-N) electron injection into the gate oxide has been a technique extensively used for characterization of degradation effects in MOS capacitors and transistors [1, 2]. It also often serves to evaluate technology-related reliability issues of MOSFETs via analysis of stress-induced damage in devices manufactured with various process recipes [3]. Such an approach, however, may result in erroneous interpretation, since PMOS and NMOS transistors behave differently during F-N stress of different polarities. In most cases, instead of expected positive shift due to electron trapping in the oxide, the negative shift, indicating an effective positive charge build-up can be observed. This behavior makes an analysis of reliability issues and process-induced damage in CMOS transistors difficult, unless the physical mechanisms responsible for degradation are understood. The trade-off between positive (hole trapping) and negative (electron trapping) charge build-up as well as the influence of interface states generation should be carefully analyzed.

## 2. EXPERIMENTAL

In order to establish the degradation mechanisms and create a consistent model, a set of measurements was performed on n+poly gate CMOS devices with 9 nm thermal oxides. Long channel (20 μm) transistors with total gate area of 400 $\mu m^2$ were chosen instead of short channel LDD devices to avoid possible spatial nonuniformity of degradation. The devices were stressed with a constant-current high field injection with drain, source and substrate shorted together. Stress voltage ($V_{FN}$) transients were monitored during F-N stress and the threshold voltage degradation was measured in stressed devices. The interface state generation was characterized by charge pumping measurements.

## 3. RESULTS AND DISCUSSION

Fig. 1. shows typical dependencies of the threshold voltage ($V_T$) shifts due to F-N electron injection in CMOS devices with very thin gate oxides. It can be clearly seen that after negative F-N stress (electrons injected from the gate) the threshold shift is much more negative, indicating larger positive effective charge. Moreover, PMOS transistors show more negative threshold shift, when compared to NMOS devices, regardless of the stress polarity.

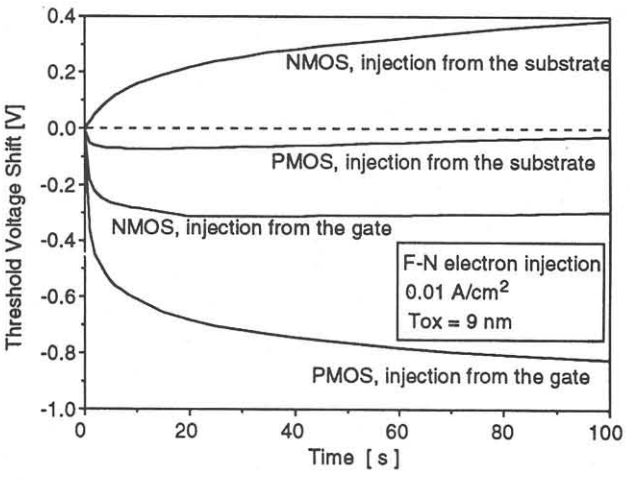


Fig. 1. Threshold voltage shift due to the F-N electron injection depends on transistor type and stress polarity.

While developing the model, the following general assumptions were made: i) oxide properties are the same in PMOS and NMOS devices and trapping and detrapping properties of bulk states in the oxide and

electron trap generation do not depend on the stress polarity; ii) during the F-N electron injection hot holes are produced in the anode and injected into the oxide [4]; iii) the initial decrease of the voltage during the stress corresponds to a positive charge build-up (hole trapping) and later, when this effect starts to saturate, an electron trapping on existing and newly generated sites becomes a dominant mechanism responsible for the increase of the stress voltage [5].

In spite of large differences in $V_T$ behavior, we observed much less variation in stress voltage changes during the stress for different devices and stress polarities (Fig. 2). One should realize, however, that these transients are recorded *during* the stress (while $V_T$ changes are measured *after* the stress) and that they reflect only the changes in the bulk charge, through modification of the energy barrier at the cathode and/or changes in the oxide field distribution.

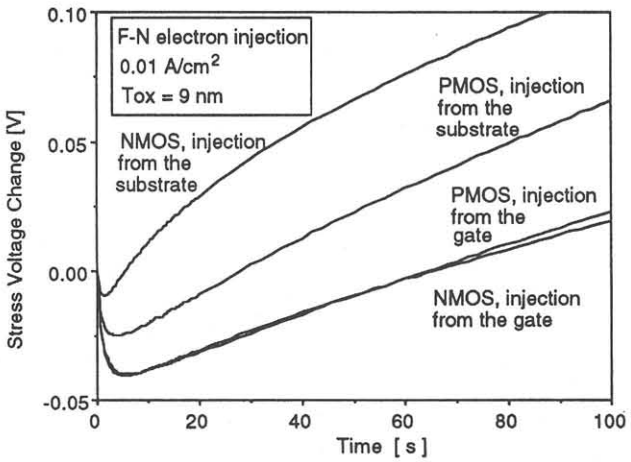


Fig. 2. Charge build-up in the oxide during the stress causes changes of the voltage needed to sustain constant current injection.

During our experiments, we have found that the first voltage transient may differ significantly from all the subsequent ones (Fig. 3), namely the voltage drop during the initial period is usually much larger in the first stress. We concluded, that part of trapped holes (assuming that a steady-state level of hole trap occupation is reached during the first F-N stress) is detrapped during the "off" time before subsequent stress or measurement, and that the emptied traps may be refilled again [6]. The nature of these traps seems to be similar to the "border traps" in the oxide [7] which can exchange the electronic charge with the silicon and which in many cases may be responsible for the so-called anomalous positive charge.

The measured dependencies of $V_T$ changes and the $V_{FN}$ transients during the F-N stresses (the first one and the subsequent, probing one) allowed us to draw conclusions about mechanisms responsible for the threshold voltage shift in CMOS transistors. The main conclusions are: i) the initial voltage drop during the first stress performed on the fresh, unstressed device is a measure of positive charge trapping in the oxide, while the initial voltage drop during the subsequent stress is a measure of hole detrapping during the "off" period between stresses; ii) hole traps are located in the vicinity of the Si-$SiO_2$ interface, mainly within the tunnelling distance; iii) energy location of hole traps in the forbidden gap of $SiO_2$ corresponds to the lower part of the Si forbidden gap, close to the top of the Si valence band; iv) newly created electron traps are distributed more or less uniformly across the oxide layer. The last conclusion is in full agreement with observations of other researchers [1, 2].

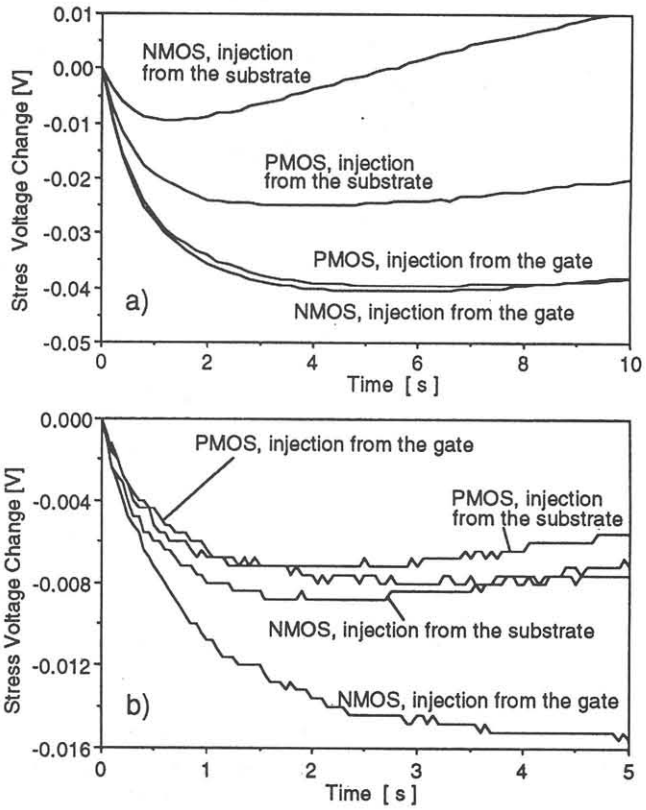


Fig. 3. Changes of the stress voltage during initial transients for the first constant current stress (a) and during the subsequent one (b).

These conclusions, along with the general assumptions made initially, served as a basis for the model proposed to explain the polarity dependence of $V_T$ degradation during F-N stress. The idea of the model is schematically presented in Fig. 4, and it relies on charge build-up during the stress and partial detrapping of holes during the "off" state after the stress, preceding $V_T$ measurements. The model takes into account the effect coming from the doping difference (band bending, work function difference) and the effect of the trapped positive charge on the potential distribution in the oxide. It can be found from Fig.4, that for the positive gate voltage stress a lower steady state level of hole trap occupation can be achieved, especially in the case of the NMOS transistor. Moreover, in NMOS devices significant number of holes may be detrapped during the post-stress "off" state. An additional effect of the bias applied during post-stress $V_T$ measurements, which in the case of NMOS transistors enhances hole detrapping, as well as the effect of charge stored at interface states (positive for PMOS and negative for NMOS devices) on $V_T$ should also be taken into account during analysis of the threshold voltage degradation. In our work we observed much stronger interface state generation in the

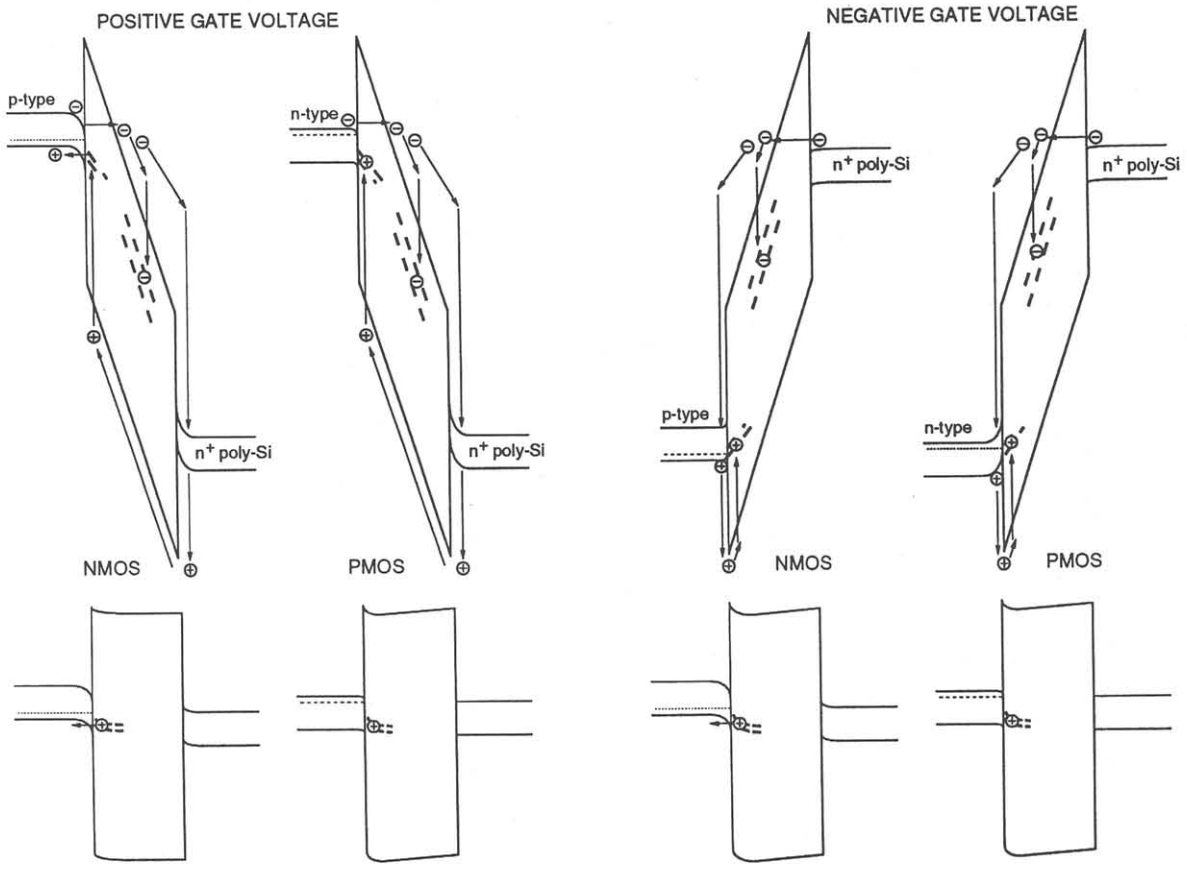


Fig. 4. Band diagram of the MOS structure showing charge trapping during F-N stress performed on NMOS and PMOS transistors, as well as detrapping of holes during the "off" period after stress.

case of NMOS devices than PMOS (Table 1), and for NMOS transistors this generation was found independent on the stress polarity. On the other hand, stress-induced increase in the interface state density in PMOS devices was higher by a factor of two for the gate electron injection than for the substrate injection.

Table 1. F-N stress-induced generation of interface states (after injection of 2 C/cm$^2$).

| PMOS, $\Delta D_{it}$ [eV$^{-1}$ cm$^{-2}$] | | NMOS, $\Delta D_{it}$ [eV$^{-1}$ cm$^{-2}$] | |
|---|---|---|---|
| F-N, $+V_G$ | F-N, $-V_G$ | F-N, $+V_G$ | F-N, $-V_G$ |
| $1.6 \times 10^{11}$ | $3.0 \times 10^{11}$ | $4.4 \times 10^{11}$ | $4.4 \times 10^{11}$ |

This observation can explain additional differences between observed threshold voltage shifts. For NMOS transistors increase of the interface state density increases the number of electrons contributing to the effective oxide charge, while for PMOS transistors it increases the number of positively ionized donor-like centers contributing to the effective oxide charge.

## 4. CONCLUSIONS

A qualitative model is proposed to explain different behavior and susceptibility of the threshold voltage of CMOS devices to F-N stress-induced degradation. The model is based on differences in charge trapping and detrapping in different regions of very thin gate oxides under different stress conditions in PMOS and NMOS transistors. The behavior of the charge trapped in the oxide has been deduced from the voltage transients during constant-current stress as well as transients during subsequent stresses. In addition to differences in the charge trapped in the oxide, interface state generation during stress make the difference between PMOS and NMOS devices more pronounced.

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