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New Experimental Findings on Stress Induced Leakage Current of Ultra Thin Silicon Dioxides

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A new degradation mode (named B mode) of Stress Induced Leakage Current (SILC) of 4nm-thick ultra thin silicon dioxides is proposed. It is shown that B mode SILC is a local area and temperature dependent phenomenon, which is different from the previous reported mode (named A mode). There is a close relationship between dielectric breakdown (time to failure) and B mode SILC (time to B mode shift). It is also shown that both dielectric breakdown and B mode shift concern with the SiO_2/Si interface roughness. Also the essential difference on the reliability evaluation between constant current and constant voltage stressing due to the existence of B mode SILC is proposed.

Introduction

Recent advance in Si MOS LSI requires ultra thin gate oxide less than 6nm. However, when the gate oxide thickness is decreased to less than 8nm, it has been shown that a Stress Induced Leakage Current (SILC) becomes a serious problem[1, 2]. Also the conduction mechanisms of SILC have been proposed[3, 4]. We have found a new mode of SILC (B mode SILC), which clearly differs from the previously reported SILC[3,4] (A mode SILC) in 4nm-thick gate oxide, that is strongly reqired in 0.1μm ruled MOS LSIs. It is shown that B mode SILC degrades the oxide reliability and relates to the SiO_2/Si interface roughness.

Experimental

MOS capacitors with 4nm-thick gate oxide and n+ polycrystalline silicon gate electrode were fabricated on CZ-P type Si (100) substrates. The current-voltage (I-V) characteristics measurement and constant voltage Fowler-Nordheim (F-N) stressing (6V:accumulation) for 50 seconds were repeatedly applied to the test devices. Also continuous constant voltage F-N stressing were performed and time to 50% failure (TTF) and time to 50% B mode shift (TTBS) were calculated with the Weibull plots. The SiO_2/Si interface roughness was analyzed by cross-sectional transmission electron microscopy (XTEM). From the XTEM photographs, root mean square of roughness, Δrms, was determined.

Results and Discussions

The results of the measured current-voltage characteristics of a MOS capacitor with 4nm-thick gate oxide film are shown in Fig. 1. After 1st cycle, A mode SILC appears, and in the next two cycles, A mode SILC increases gradually. After the next cycle as shown in

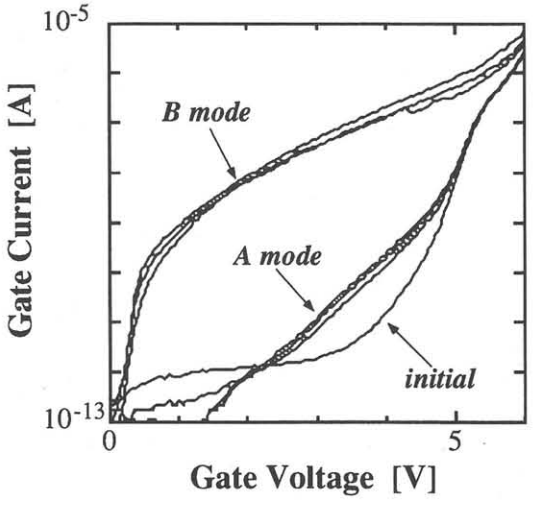

Fig. 1 Typical current - voltage characteristics of a MOS capacitor with 4nm-thick oxide film, showing A mode and B mode SILCs (stress induced leakage current) by repeated F-N stress.

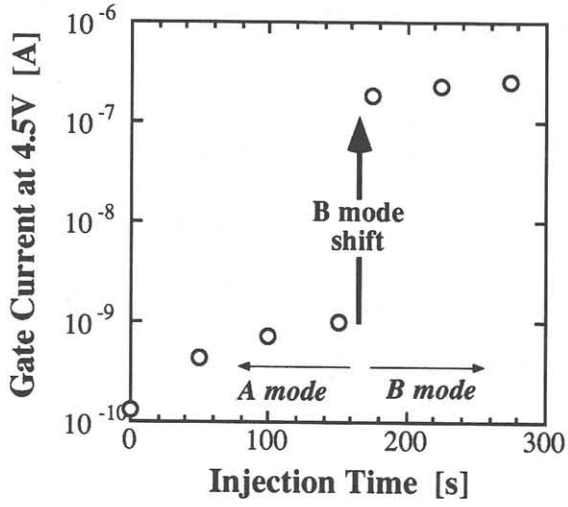

Fig. 2 The change of gate current at 4.5V by constant voltage F-Nstressing. B mode SILC doesn't depend on injection time, while A mode SILC increases as a function of it.

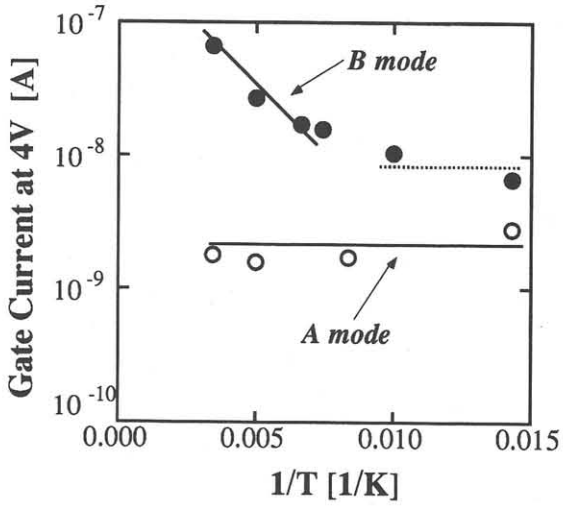

Fig. 3 Arrhenius plots of A mode and B mode SILCs. Only B mode has the temperature dependence.

Fig. 2, the gate current increased by 2 order within just 1 second. We determine this phenomenon as B mode shift. After the B mode shift, B mode SILC doesn't increase clearly. This shift is not dielectric breakdown, because at higher field range more than 6V, F-N tunneling current is observed.

The Arrhenius plots of A and B mode SILCs are shown in Fig. 3. B mode SILC depends on temperature at the regime higher than 120K, while A mode SILC shows no temperature dependence. These results show that the conduction mechanisms of A and B mode SILCs are different each other.

The current-voltage characteristics including B mode SILC of the capacitors with three different gate areas are shown in Fig. 4. It is clear that B mode SILC is independent on the gate area of capacitor in the case of the area larger than 0.01mm^2. So, B mode SILC is considered to be a local area phenomenon.

The change of gate current during constant voltage F-N stress was shown in Fig. 5. Three steps of B mode shift were occurred before breakdown in this sample. We often observed such multi-step B mode shifts. When the stress voltage becomes higher, multi-step B mode shift becomes not distinguished.

Next, four samples fabricated with different process conditions were tested under constant voltage stress. The interface roughness (Δrms) was estimated from two XTEM photographs for each sample. The relationship between Δrms and TTF, TTBS was shown in Fig. 6.

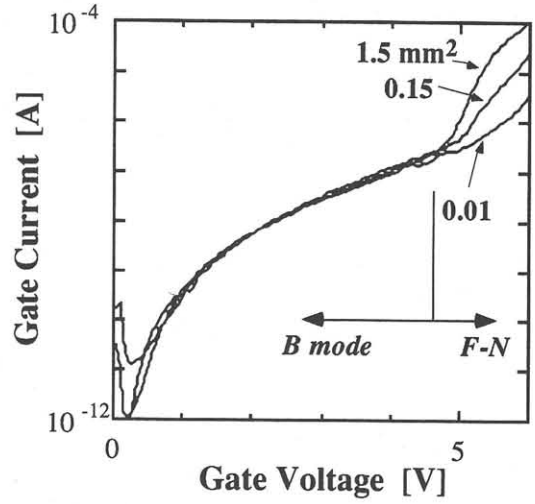

Fig. 4 The gate area (1.5, 0.15, 0.01mm^2) dependence of B mode SILC, showing B mode SILC does not depend on the area.

Clear relationships were observed between Δrms and both TTBS and TTF. The ratio of TTF and TTBS becomes smaller as Δrms increases and TTF decreases. We have already reported that the interface roughness of SiO_2/Si has a local maximum when oxide thickness is about 4nm in the ordinary process[5, 6] It has been also reported that the electron channel mobility in MOSFET is strongly dominated by the interface roughness[7]. These results mean that it is strongly

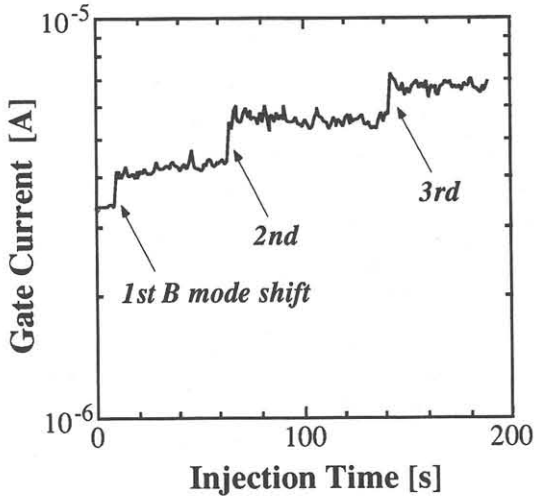

Fig. 5 The multi-step B mode shift during F-N stressing. In this sample, three degradation steps were occured before breakdown.

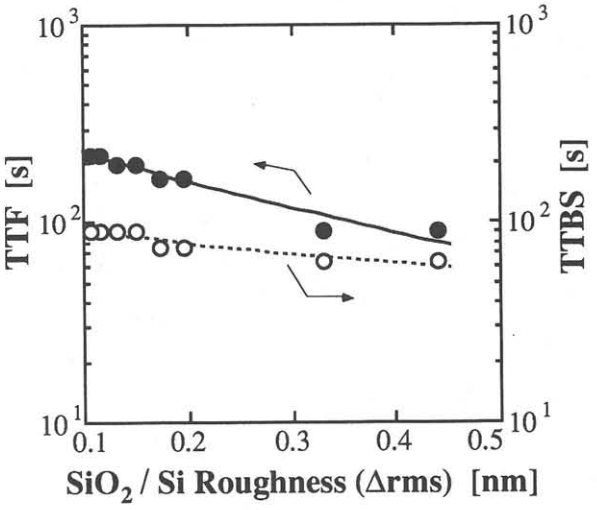

Fig. 6 Relationship between SiO_2/Si interface roughness (Δrms) and time to failure, time to B mode shift of four different samples.

required to smooth the interfaces to achieve ULSI with 4nm-thick gate oxides. It is also suggested that we may not evaluate the real thickness dependence of the oxide reliability, because of the thickness dependence of the interface roughness[5, 6].

Considering the dependence of B mode SILC on the gate area (Fig. 4), multi-step B mode shift (Fig. 5) and the relationship between the interface roughness and TTF, TTBS (Fig. 6), B mode SILC is considered to be as follows: B mode shift occurs at local area, *i.e.*, weak spot, at first. The first shifted spot is not always become the breakdown spot. Before breakdown, some B mode shifts occur at weak spots, which relate to the interface roughness. The number of steps of B mode shift before breakdown depends on the oxide quality including interface roughness and stress condition. At higher stress condition, the probability that the breakdown occurs at the spot where the first B mode shift occured becomes higher.

Furthermore, these results suggest the essential difference on the reliability evaluation in ultra thin oxides between constant current and constant voltage stressing. As described above, multi-step B mode shift occurs in constant voltage stressing before oxide breakdown. In contrast, multi-step B mode shift is difficult to occur by constant current stressing because of the lowering of the effective field by B mode SILC. Hence, the reliability for the constant current stress is more enhanced than the constant voltage stress.

Conclusion

A new degradation mode, B mode SILC, in 4nm-thick oxides is proposed. This mode is very important for the reliability degradation of ultra thin gate oxides also for the reliability evaluation. Furthermore, the influence of the SiO_2/Si interface roughness to the oxide integrity is clarified.

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