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The Impact of Nitrogen Implantation into Highly Doped Polysilicon Gates for Highly Reliable and High Performance Sub-Quarter Micron Dual Gate CMOS

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We studied the effects of nitrogen implantation into highly doped polysilicon gates for sub-quarter micron CMOS in detail. The current drivability of MOSFETs can be improved by highly doped polysilicon gates. However it was founded that highly arsenic doped polysilicon gates caused a degradation of gate oxide film and highly boron doped polysilicon gates resulted in a shift of threshold voltage by boron penetration. The nitrogen implantation into polysilicon gates can effectively overcome these problems. Moreover, the hot carrier resistance can be also improved by nitrogen implantation. Therefore, we can achieve highly reliable and high performance dual gate CMOS using the newly developed process.

1. Introduction

There has been increasing attention on the improvement of performance for sub-quarter micron CMOS. Dual gate structure using the surface channel MOSFETs has been widely employed to suppress short channel effect of PMOSFETs.[1] However, the gate polysilicon depletion, which causes threshold voltage shift by increase in effective oxide thickness and reduction of the electric field in the gate oxide, is one of major issues for dual gate operation.[2,3] Moreover hot carrier degradation will be a major issue, although supply voltage is lowered down to 2.5 V for 0.25 μm MOSFETs. Recently, we proposed novel structure using nitrogen implantation into polysilicon gates for nitrided oxide formation to improve the reliability of MOSFETs.[4,5] The target of our investigation in this paper will aim at highly reliable and high performance sub-quarter micron dual gate CMOS.

2. Experimental

Figure 1 shows the schematic cross-section of newly developed dual gate CMOS using nitrogen implantation into polysilicon gates. Before gate electrodes definition, nitrogen ions were implanted into the polysilicon film for the nitrided oxide formation. Subsequently, arsenic ions and boron ions were implanted to form N^+ gates and P^+ gates, respectively. The dopant concentration of polysilicon gate was changed to evaluate the effect of the degeneracy level of polysilicon gates. The thickness of gate oxide film was 6 nm.

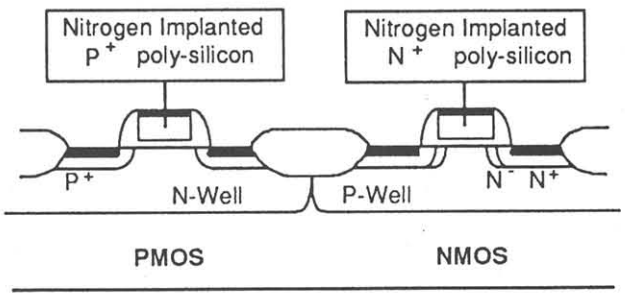

Fig. 1 The schematic cross-section of dual gate CMOS with nitrogen implanted gates.

3. Results and Discussion

Figure 2 presents the dependence of normalized capacitance of N^+ polysilicon gate capacitors on arsenic dose into polysilicon gates with nitrogen dose as a parameter. The normalized capacitance decreases with decrease in arsenic dose due to the depletion layer formation in the gate electrode. Almost no change of activation rate can be observed by nitrogen implantation. Figure 3 gives drain current of 0.25 μm NMOSFETs for the same samples shown in Fig. 2. Low-doped gate has low drain current due to increase in threshold voltage and decrease in transconductance caused by depletion layer formation at the SiO2/polysilicon interface. Therefore highly doped polysilicon gates are necessary for high drivable MOSFETs. Figure 4 gives the effects of the arsenic concentration on constant current TDDB characteristics. The injection is performed from substrate at the current density with -0.1 A/cm^2. The random failures of oxide films increase with increase in arsenic dose. The deterioration of gate oxide films under highly

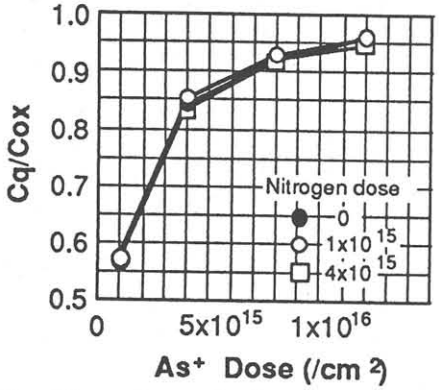

Fig. 2 Dependence of normalized capacitance on arsenic dose into polysilicon gates with nitrogen dose as a parameter.

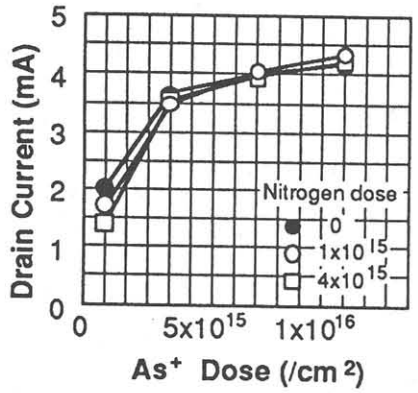

Fig. 3 Drain current of 0.25 μm NMOSFETs for same samples shown in fig. 2 (Vd= Vg=2.5V).

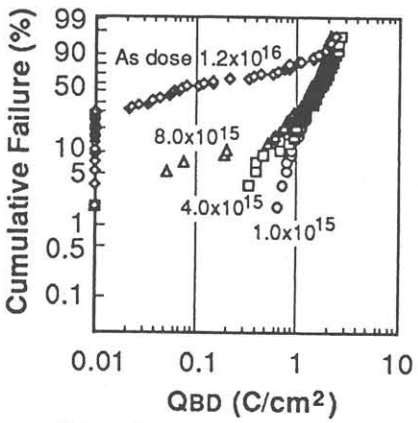

Fig. 4. Characteristics of constant current TDDB of N^+ gate capacitor on arsenic dose.

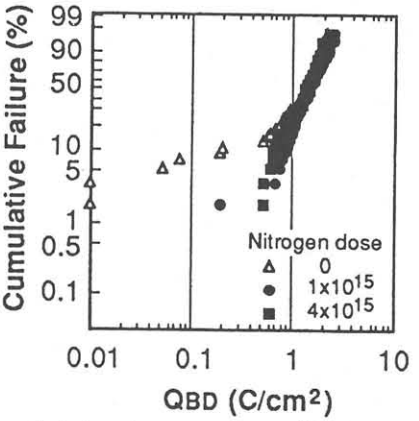

Fig. 5. Characteristics of constant current TDDB of nitrogen implanted N^+ gate capacitor. Arsenic dose is 8.0×10^{15} /cm^2

doped gate capacitor can be minimized by nitrogen implantation as shown in Fig. 5. Figure 6 depicts the SIMS depth profiles of impurities in the N^+ polysilicon gate and the gate oxide film with and without nitrogen implantation. It should be noted that the pileup of nitrogen into gate oxide film from polysilicon gate can be clearly observed with nitrogen implanted sample. At the same time, the segregation of arsenic into the gate oxide film can be reduced. The hot carrier degradation for 0.25 μm NMOSFETs is shown in Fig. 7, where the threshold voltage shift by DAHC (Drain Avalanche Hot Carrier) injection is evaluated under the gate voltage giving the maximum substrate current. The hot carrier resistance can be improved by nitrogen implantation. The generation of interface states and electron traps can be reduced by nitrogen implantation. The improvement of hot carrier degradation against CHE (Channel Hot Electron) injection can be also observed.

Figure 8 shows normalized capacitance for P^+ polysilicon gate capacitor. The depletion layer formation in the gate electrode can be suppressed with increase in the boron dose as well as the case of N^+ gate capacitor. Therefore the saturation current of highly doped P^+ gates MOSFET can be increased to suppress the increase in the effective oxide thickness. There is no significant change of the degeneracy level of polysilicon in highly doped gate by nitrogen implantation, while gate polysilicon depletion by nitrogen implantation can be observed for low-doped gates. Figure 9 shows dependence of the flatband voltage shift on boron dose into polysilicon gate. The flatband voltage shift caused by boron penetration through gate oxide film into silicon substrate can be distinctly observed for highly boron doped gates. The nitrogen implantation can effectively suppress the boron penetration. The segregated nitrogen into the gate oxide film can act as a barrier layer for the boron diffusion. The hot carrier resistance of PMOSFET can be also improved by nitrogen implantation.[5] Therefor, highly reliable and high performance p^+ gate PMOSFET can be realized by nitrogen implantation.

The propagation delay time of CMOS ring oscillator with 0.25 μm gate length is plotted in Fig. 10. The delay time of 0.25 μm CMOS with highly doped gate is 30 % faster than that with low doped gate at the supply voltage of 2.5 V. The increase in the saturation current and the lower threshold voltage are main reasons for the superior circuit performance. Moreover, the delay time with low-doped gates rapidly increases at the lower supply voltage due to the high threshold voltage.

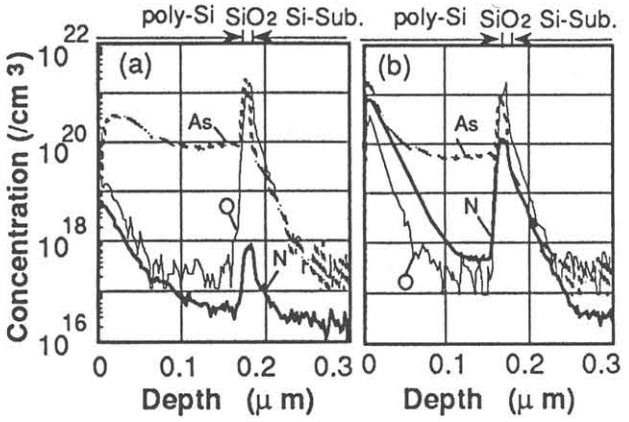

Fig. 6 SIMS depth profiles of As,N,O in poly-Si gate and gate oxide measured on samples without nitrogen implantation (a), and with nitrogen implantation at a dose of $8x10^{15}/cm^2$ (b). As dose is $4x10^{15}/cm^2$.

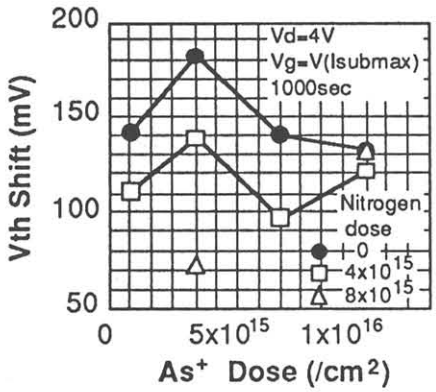

Fig. 7 Dependence of Vth shift of 0.25 μm NMOSFETs under DAHC injection.

4. Conclusion

We studied the effects of nitrogen implantation into highly doped polysilicon gates in detail. The current drivability of MOSFETs can be improved by highly doped polysilicon gates. However it was founded that highly arsenic doped polysilicon gates caused a degradation of gate oxide film and highly boron doped polysilicon gates resulted in a shift of threshold voltage by boron penetration. The nitrogen implantation into polysilicon gates can effectively overcome these problem. The nitrogen implanted into polysilicon gate is segregated into the gate oxide film during the heat treatment after implantation. The nitrogen into gate oxide film can act as a diffusion barrier for boron penetration and reduce the random failures of gate oxide film. Moreover, the hot carrier resistance can be also improved by nitrogen implantation. This improvement should be due to the reduction of interface states generation and electron trap formation. Our extensive investigations conclude that highly reliable and high performance dual gate CMOS can be realized by nitrogen implantation.

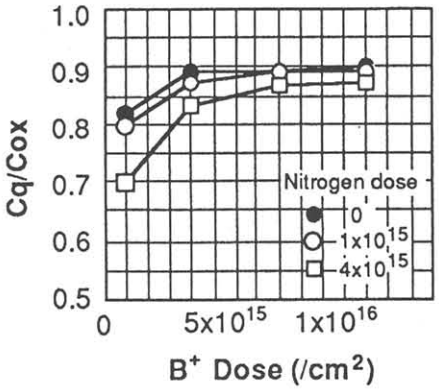

Fig. 8 Dependence of normalized capacitance of PMOSFETs on boron dose with nitrogen dose as a parameter.

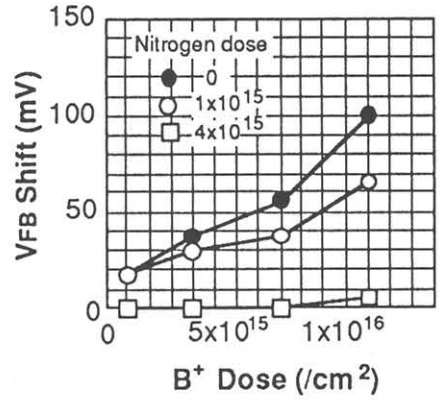

Fig. 9 Vfb shift of PMOSFETs for same samples shown in fig.8

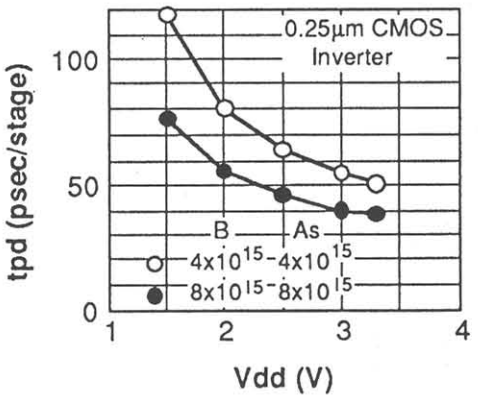

Fig. 10 Delay time of 0.25 μm CMOS ring oscillator with supply voltage as a function of gate doping level.

5. Acknowledgment

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