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Reducing the Reverse-Bias Current in 450°C-Annealed n^+p Junction by Hydrogen Radical Sintering

M. M. Oka, A. Nakada, K. Tomita, T. Shibata, T. Ohmi, T. Nitta*

Department of Electronic Engineering, Faculty of Engineering, Tohoku University,
Aza-Aoba Aramaki Aoba-ku, Sendai 980-77, JAPAN
*Device Development Center, Hitachi Ltd., Oume-shi, Tokyo, JAPAN

Ultra-shallow n^+p junctions featuring very low reverse-bias current densities (3.1×10^{-9} A/cm^2 at -5 V) have been successfully formed at a post-implantation annealing temperature as low as 450°C. Such a low reverse-bias current level has been achieved by eliminating residual point defects remaining after 450°C post-implantation annealing by a newly developed hydrogen radical sintering (H^*-sintering).

1) INTRODUCTION

There is a strong interest in forming low reverse-bias current junctions at low temperatures (e.g., 450°C) because the establishment of total low temperature processing (below 500°C) is an essential requirement for implementing metal substrate CMOS devices, which are expected to operate at frequencies as high as 10 GHz[1]. Previously we succeeded in reducing the reverse-bias current of ion-implanted n^+p junctions by low temperature annealing. This was achieved by using a UHV ion implanter[2] to eliminate residual gas contamination, and also by installing silicon protecting covers over metal internal components of the ion implanter **(Fig.1)** in order to eliminate metal contamination caused by high energy ion beam sputtering[3]. However, junctions formed at 450°C so far have presented reverse-bias current levels about two orders of magnitude higher than samples formed at 1000°C, so that sources of leakage current other than residual gas-molecule adsorption and metallic sputtering contamination must be investigated.

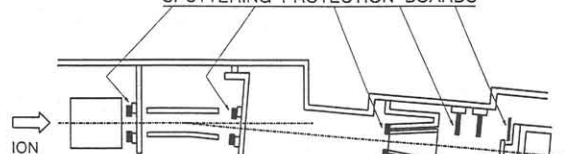

Fig.1) Schematic of the location of silicon boards installed in order to avoid sputtering caused by high energy ion beam in the UHV ion implanter.

Sintering in forming gas ambient is widely accepted as a process to reduce the interface trap density[4, 5]. It is proposed that hydrogen atoms can passivate electrically active traps existing at the interface between Si and SiO_2. However, numerous papers have shown that annealing in molecular hydrogen ambient at temperatures below 600°C result in little H penetration into the bulk of Si[6]. The classic H penetration measurement by Wieringen and Warmoltz[7] showed a very low hydrogen solubility in Si (around 10^{15} cm^{-3} at 1 atm at 1200°C), giving support to the observation. Consequently, there is no report about passivation of traps existing in the bulk of the Si by sintering in H-containing ambient.

However, the rather large value of the hydrogen diffusivity in Si (around 10^{-10} cm^{2}s^{-1} at room temperature[7]) can provide a large number of hydrogen molecules penetrating through the bulk of Si, thus might give chance to terminate traps in Si. The fact that no trap passivation effect has been so far observed suggests that molecular hydrogen has a very low reactivity with traps located in the bulk of Si. It is proposed in this work that sintering in an ambient containing hydrogen radicals (H^*) instead of molecular hydrogen can reduce the density of traps in the midgap existing in the bulk of Si.

2) EXPERIMENTAL PROCEDURE

The n^+p diodes were formed by implanting As at 25 keV with a dose of 2×10^{15}cm^{-2} to p-type, (100) Si substrates of 4.5-6.0 Ωcm resistivity. The annealing of ion-implanted layers was carried out in nitrogen ambient at varying temperatures ranging from 450°C to 1000°C. All diodes were subjected to sintering in a forming gas ambient at 400°C for 20 min. H^*-sintering was carried out in a specially designed furnace, which is schematically presented in **Fig.2**. The furnace is made of 0.5 m long Hasteloy tube with an internal diameter of 30 mm. A gas mixture of 10%H_2/90%Ar was fed to the furnace through a 4 m long Ni tube with an

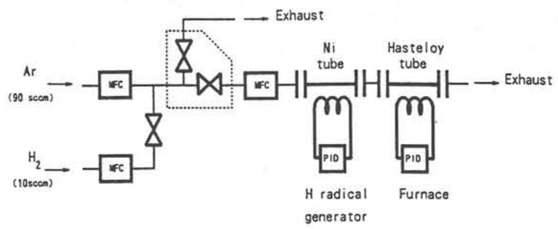

Fig.2) Schematic of the furnace designed to carry out the hydrogen radical sintering.

internal diameter of 3 mm. Both Hasteloy and Ni act as catalyst for hydrogen radical formation. Both tubes can be independently heated but in our particular case they were set at the same temperature. The H^*-sintering was carried out in two steps, namely at 450°C for 20 min and than at 420°C for 3 h.

3) RESULTS AND DISCUSSION

The reverse-bias current obtained by post-implantation annealing at 450°C, even without H^*-sintering, is three to four orders of magnitude lower than the previously reported data[8, 9], as shown in **Fig.3**. Therefore, our diodes are very sensitive to low-level defects, thus being suited to study the behavior of residual defects in low-temperature annealed junctions.

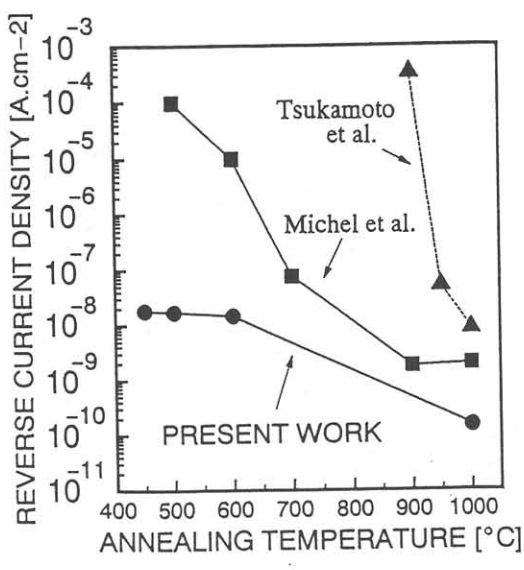

Fig.3) Reverse-bias current density measured at –5 V as function of the annealing temperature compared with previously reported data[8, 9].

In **Fig.4** the current densities are shown as a function of the applied bias for different annealing temperatures. It is observed that not only the reverse-bias current but also the forward-bias current increases as the post-implantation annealing temperature is decreased. The reverse-bias current

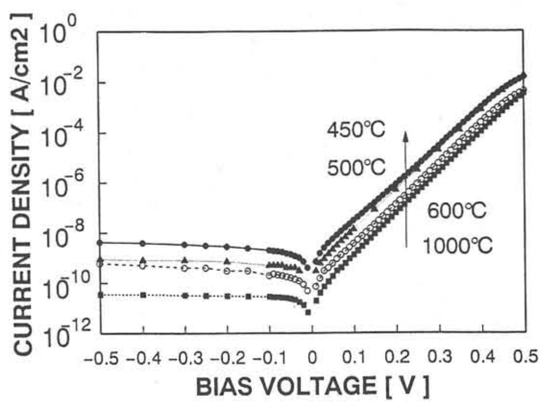

Fig.4) Current-voltage characteristics measured for n^+p junctions formed by 450°C, 500°C, 600°C and 1000°C post-implantation annealing.

of junctions annealed at low temperatures is governed by the carrier generation in the depletion region. Therefore, the increase in the current density is attributed to the residual defects generated by ion implantation, which increase as the annealing temperature is reduced. Thus, the behavior of the reverse-bias current is quite reasonable. On the other hand, however, the forward-bias current is governed by the diffusion of electrons (recombination current) in the neutral p-type region. Thus, it depends on the properties of the p-type substrate not in the vicinity of the implanted region. Therefore, it is hard to believe the forward-bias current increases depending on the annealing temperature. The present result indicates the existence of a strong relationship between the forward- and reverse-bias currents in our samples, suggesting the ion-implantation induced damages are present in the region of p-type substrates that determine the forward current.

In particular, comparing the samples annealed at 450°C and 1000°C, it is seen that the current density increases by about two orders of magnitude when a reverse bias is applied, while one order of magnitude increase is observed when a forward-bias is applied, i.e., there is a quadratic relation between the two values. Considering the expressions of the reverse- and forward-bias current densities, J_R and J_F, respectively, as given in **Fig.5**, we can see that J_R is inversely proportional to the generation lifetime (τ_{gen}), while J_F is inversely proportional to the square root of the recombination lifetime ($\sqrt{\tau_{rec}}$). From these facts, we can infer that the generation lifetimes and the recombination lifetimes have the same dependence on annealing temperature.

In **Fig.5** both lifetimes normalized to the respective lifetimes measured at 1000°C are plotted as a function of annealing temperature. The generation lifetime was calculated from the reverse-bias current at –0.5 V and the recombination lifetime from the forward-bias current at 0.3 V. Both lifetimes fit very well on a single curve. This result gives support to the assumption made above.

It is well known that defects generated by ion implantation process cannot be completely annealed out even by high-temperature post-implantation annealing. We speculate that the degradation of the lifetimes is caused by defects

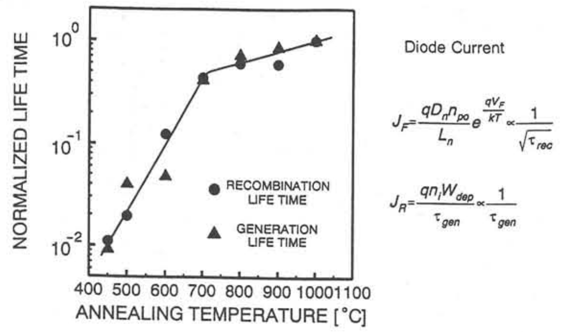

Fig.5) Generation and recombination lifetimes of samples annealed at various temperatures normalized to the respective values measured after 1000°C jointly with the formulas of reverse- and forward-bias currents.

remaining in Si after the post-implantation annealing, and that the same defects are responsible for determining both generation and recombination lifetimes since they present the same temperature dependence. We propose also that these defects are distributed into a considerably deep region in the bulk of silicon. This assumption is supported by two facts: firstly, the generation current continuously increases with the application of a reverse bias voltage (the depletion layer width at –5 V is about 1.6 μm), and secondly, the diffusion current (forward–bias current) increases in accordance with the increase in the generation current (reverse–bias current) when annealing temperature is reduced. This indicates that the bulk silicon, the region outside the depletion layer, is also affected by the ion implantation. Secondary defects are known to grow toward the surface and not toward the bulk[10]. Therefore it is reasonable to suppose that the defects that govern the presently described phenomena are highly mobile point defects created by ion implantation, which have diffused deep into the wafer.

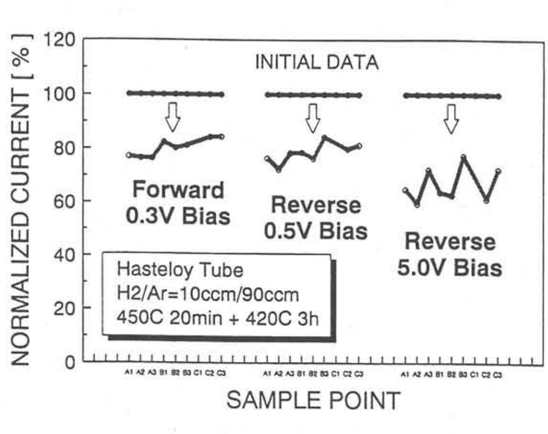

Fig 6) Current densities measured after H^*–sintering of 450°C/20 min followed by 420°C/3 h normalized to the values measured before this sintering. Measurements were made at a forward bias of 0.3 V and at reverse bias of –0.5 and –5 V.

It is expected that such point defects deep–distributed in the Si substrate can be terminated by H^*–sintering. H^*–sintering carried out at 450°C, however, did not show any improvement in the diode characteristic. Presumably, the H^*–sintering temperature of 450°C is too high to stabilize the termination of point defects. Then, the H^*–sintering was carried out at 420°C for 3 h. Reduction in the reverse–bias current by 20–30% was observed, as shown in **Fig.6**. The figure shows the current densities measured after the H^*–sintering normalized to the values before the sintering process. The use of H^*–sintering permitted us to lower the reverse–bias current level at -5 V down to 3.1×10^{-9} A/cm^2. It is noteworthy that samples sintered in forming gas at the same temperature did not present any improvement in the reverse–bias current level. Optimization of H^*–sintering conditions is presently in progress and more significant improvements are yet expected.

5) CONCLUSION

It has been shown that H^*–sintering at 420°C for 3 h is effective in reducing the reverse–bias current by 20 to 30% compared to the values before the sintering. This sintering has been proposed by the assumption that one source of excessive currents of the junction annealed at low temperature are point defects produced during the ion implantation, deep distributed into the bulk Si, which could not be completely annealed out by post implantation annealing at low temperature. The reverse–bias current at 5 V has been reduced to a value as low as 3.1×10^{-9} A/cm^2 by the present technology.

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