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Concave-DMOSFET: A New Super Low On-Resistance Power MOSFET

Norihito TOKURA, Tsuyoshi YAMAMOTO, Mitsuhiro KATAOKA,
Shigeki TAKAHASHI and Kunihiko HARA

Research and Development Dept., Nippondenso Co., Ltd.
1-1 Showa-cho, Kariya-city, Aichi-pref. 448 Japan

A new super low on-resistance power MOSFET is presented. The new transistor "Concave-DMOSFET" has a concave channel structure fabricated not by trench etching technique, but by a combination of local oxidation of silicon (LOCOS) and diffusion self alignment (DSA) using oxide film as a double diffusion mask. The Concave-DMOSFET based on 16μm cell design has been fabricated for the first time, and the specific on-resistance of 75m$\Omega \cdot mm^2$ with breakdown voltage of 50V has been achieved. This value is the lowest ever reported for power MOSFETs of comparably same design rule.

1. INTRODUCTION

A specific on-resistance (R_{SP}) of low-voltage planar-DMOSFET has been significantly reduced by decreasing microcell pitch. But, the optimum value of the pitch providing lowest R_{SP} exists between 10 and 15 μm[1-2]. This is because JFET resistance (r_{JFET}) increses in accordance with scaling down of cell pitch and becomes dominant component of on-resistance. A trench-DMOSFET, in which r_{JFET} component is eliminated, has overcome planar-DMOSFET in R_{SP}[3]. However, sharp corners of trench structure degrade device breakdown voltage (BV_{DS}), and trench-DMOS process including reactive ion etching (RIE) has not been controlled sufficiently yet[4]. Some RIE damage is left on the trench walls through ion etching process, and the damage results in degradation of channel mobility[5].

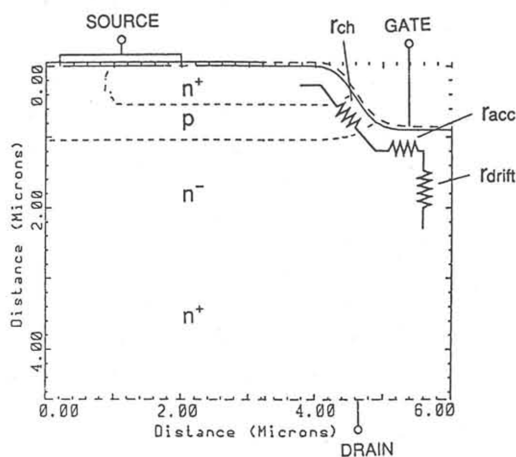
A concave structure can be formed by LOCOS technique[6]. Therefore LOCOS process is expected to solve the problem of trench-DMOS process such as sharp corners on the wall. And we have shown fundamental feasibility study of LOCOS based new DMOS technology by means of numerical simulation[7].

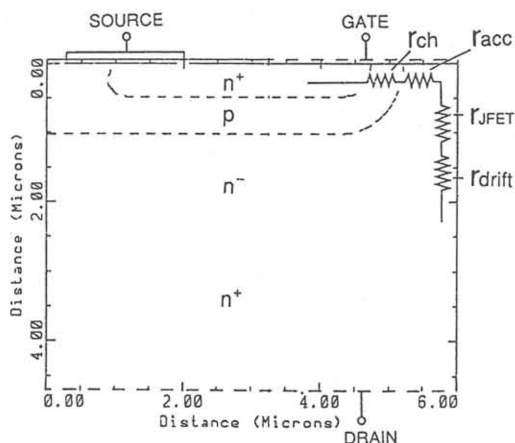
We have successfully developed new low on-resistance power MOSFET based on LOCOS process for the first time, and it was named as Concave-DMOSFET by the authors. In this paper, we will show the features and characteristics of fabricated Concave-DMOSFET.

2. DEVICE SIMULATION

Fig.1 shows 2-D device simulation model of half unit cell of n-channel Concave-DMOSFET compared with that of planar-DMOSFET. Cell pitch was selected as 12μm, because it was nearly the optimum value of minimum R_{SP} of planar-DMOSFET. Device parameters of Concave-DMOSFET were equal to optimized those of planar-DMOSFET except for concave structure. The concave structure eliminates r_{JFET}, which is the main component resistance in planar-DMOSFET, and reduces the R_{SP} of Concave-DMOSFET drastically.

According to our simulation, R_{SP} was 50m$\Omega \cdot mm^2$ for Concave-DMOSFET and 80m$\Omega \cdot mm^2$ for planar-DMOSFET under the conditions of gate voltage (V_{GS}) and drain voltage (V_{DS}) being 10V and 0.6V. The threshold voltage (V_{TH}) and BV_{DS} were 1.8V and 52V for both models. From these simulated results, R_{SP} of Concave-DMOSFET was estimated as about 40% lower than that of planar-DMOSFET.





(a)Concave-DMOSFET(R_{SP}=50m$\Omega \cdot mm^2$)　　(b)planar-DMOSFET(R_{SP}=80m$\Omega \cdot mm^2$)

Fig.1 Device simulation models of half unit cell. Cell pitch is 12μm. The r_{ch}, r_{acc}, r_{JFET} and r_{drift} are channel, accumulation, JFET and drift resistance respectively. The structure of Concave-DMOSFET eliminates r_{JFET} and reduces the on-resistance. BV_{DS} is 52V for both models.

3. EXPERIMENTS

A (100) oriented silicon wafer which had n^- epi-layer with $1\times10^{16}cm^{-3}$ phosphor doping was used as a substrate. First of all, Si_3N_4 film was deposited as an local oxidation mask. After patterning of Si_3N_4 film, oxidation of silicon was carried out in order to form the concave structure of 0.9μm depth. Then, double diffusion (DSA) using LOCOS SiO_2 mask and 0.5μm channel were formed along side surface of the concave. After removing LOCOS SiO_2 film, gate oxide and electrode were successively formed. Finally, source and drain electrode were formed by conventional evaporation technique.

Fig.2 shows a cross sectional view of fabricated 16μm$\times$16μm square unit cell. In the figure, depth and width of the concave are 0.9μm and 4μm respectively. Side wall surface of the concave is (111) oriented. Gate oxide film of 60nm thickness uniformly covers the concave surface. Fig.3 shows the picture of the fabricated Concave-DMOSFET chip in which 13135 cells are integrated, and its active area (S_A) is 3.36mm^2.

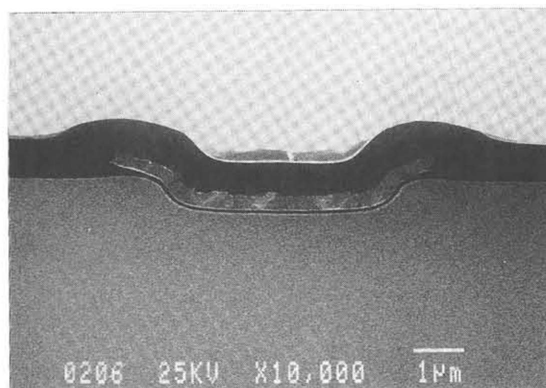


Fig.2 A SEM photomicrograph of cross sectional unit cell structure of fabricated Concave-DMOSFET.

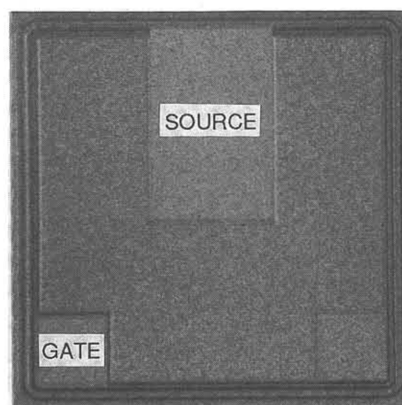


Fig.3 A picture of the 2.5mm$\times$2.5mm Concave-DMOSFET. 13135 cells are integrated. Unit cell pattern is 16μm$\times$16μm square.

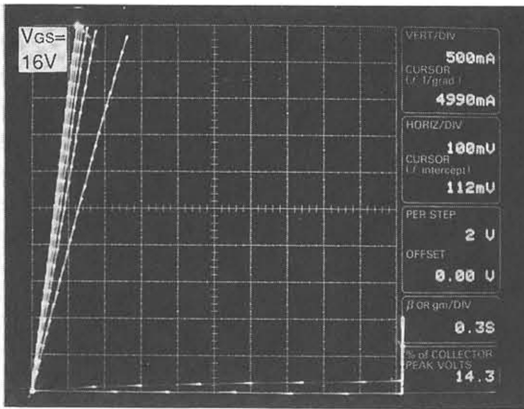


Fig.4 I-V characteristics of the Concave-DMOSFET. Specific on-resistance is 75m$\Omega \cdot mm^2$ (V_{GS}=16V).

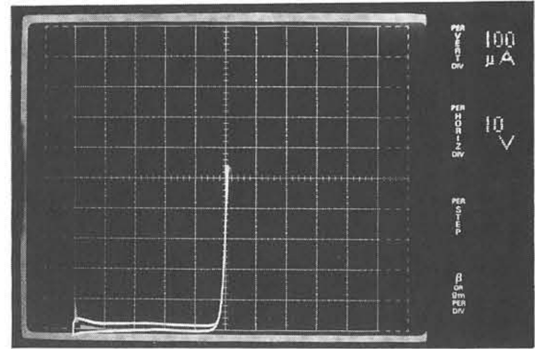


Fig.5 Breakdown characteristics of the Concave-DMOSFET. Breakdown voltage is 50V.

4. RESULTS AND DISCUSSION

I-V characteristics of linear region is shown in Fig.4. From the operating point (112mV,4990mA) on the line of V_{GS}=16V, R_{SP} calculated by $(V_{DS}/I_D)*S_A$ was 75m$\Omega \cdot mm^2$. Under the condition of V_{GS}=10V, R_{SP} was 85m$\Omega \cdot mm^2$ given by the same way, and the value is good agreement with R_{SP} of 89m$\Omega \cdot mm^2$ estimated by the same simulation for 16μm cell pitch model. V_{TH} was 1.2V, which was lower than 1.8V of the device simulation. Drain breakdown characteristics is shown in Fig.5. BV_{DS} was measured as 50V, which was reasonably equal to simulated value.

Effective mobility of the channel was 260cm^2/V·s under the condition that electric field in gate oxide was 1MV/cm. This value is comparably high with that of planar-DMOSFET.

5. CONCLUSION

We demonstrated a new super low on-resistance power MOSFET, named as Concave-DMOSFET, which realizes drastic R_{SP} reduction of 40% compared with conventional planar-DMOSFET. The Concave-DMOSFET has been successfully fabricated for the first time and achieved the lowest R_{SP} of 75m$\Omega \cdot mm^2$ for 16μm cell power MOSFETs. The lowest R_{SP} has been realized by means of Concave-DMOS technology, which eliminates R_{JFET} and provides damage less concave surface resulting high channel mobility.

Concave-DMOSFET promises a great improvement in power loss of power MOSFETs operated under high power switching.

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