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Studies on the Process and Characteristics of 8×4cm² Silicon Microstrip Sensors

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A proto type $8x4cm^2$ silicon microstrip sensor has been designed and fabricated successfully. In order to get good quality capacitor, ONO (Oxide-Nitride-Oxide) is used to replaced the usual SiO₂ layer as the dielectric of coupling capacitor. Some gettering technologys having Boron solid source diffusion process have proposed to prevent the implant damage caused by p+ strip process. From the studies of electrial measurement and beam test, the proposal sensor has been found to have very good performance.

1. INTRODUCTION

The advantage of using silicon detector are not only for its high-precision spatial resolution but also for its low working voltage. Many existing and future high energy experiments are proposed to construction of large area silicon trackers based on mircorstrip sensors. The AC coupling readout scheme is often chosen to cope with amplifier saturation due to the leakage current. (1) (2) Usually, the coupling capacitor is made by separating the p+ strip from the readout metal strip with a thin layer of silicon dioxide. Production yield and breakdown voltage of the large area coupling capacitor is still the major problem in the recent study.(3) In addition, in order to reduce the leakage current and increase the S/N (signal-to noise) ratio, some technologys have been widely studied. (4) (5) This report presents results of our studies related to the above mentioned points.

2. DESIGN

The mask set of single-sided single-metal silicon microstrip sensor consisted of 4 layers. these masks defined p+ strip, polysilicon, contact hole and metal strip. The micorstrip sensor consists of diode strips with 2.5 um pitch, in which the readout pitch was 50um. Each diode was connected to a bias line by an individual polysilicon biasing resistor. The coupling of the metal to the diode was capacitive via a multilayer dielectric - ONO. Due to the nearly pinhole - free characteristics voltage and production yeild rate of ONO capacitor, it is expected to have higher capacitance than those of the usual oxide capacitor. The connecting line was ended in a bonding pad of 70x200cm². Each end of the active area was the connection zone for the high resistance polysilicon biasing resistor connected to a metal strip which provided the bias for diodes. The polysilicon resistor were designed to let all strips should have the same equal resistivity.

3. PROCESSING AND ELECTRICAL MEASUREMENTS

The process flow of the proposed $8x4cm^2$ silicon microstrip sensor is shown in Fig.1. A 4 K Ω -cm n-type (111) silicon wafer with $320\pm15um$ thickness was used as the substrate. The first mask defined the p+ strip pattern which extended over the active area and the guard ring. The second mask defined the polysilicon bias resistors. The third mask was used to open contact holes, and the last one defined the metal pattern which ran over the p+ strip, connecting lines and bonding pad.

Fig.1. Mask layout for single metal process.



Intrinsic gettering Isolation oxidation \downarrow P+ strip pattern define \downarrow P+ strip imp. \downarrow Poly resistor forming ONO capacitor growth \downarrow Extrinsic gettering \downarrow Contact hole open \downarrow Metal strip process \downarrow Backside metal sputter \downarrow Alloy

Fig.1. Process flow of 8x4cm² silicon microstrip sensor

From the results of electrical measurement, the following modification of process had been introduced:

(a). The multilayer dielectric - ONO was chosen to replace oxide layer in the coupling capacitor. Due to the characteristics of multilayer dielectric, the breakdown voltage of ONO capacitor was much higher than that of the oxide capacitor, and

the production yield is also much higher. The capacitor test patterns consist of oxide or ONO layer sandwiched by aluminum read out electrode and P+ strip had been test to study those effects.

The result is shown in Fig. 2. Most of the SiO^2 samples brokedown at voltage around 100-140 volts,

closed to the experience value 6-7 MV/ μ m. Some of the oxide test pattern brokedown around 0.1-40V, which was probably due to a pin hole or staking fault. In comparison, all 200 ONO samples passed 200V without breakdown.

The ONO capacitors, breakdown voltage of $2 \times 2 \text{ cm}^2$

sensor were higher than 200V and those for $8 \times 4 \text{ cm}^2$ sensor were around 160V. And tests over 10 batches (200 wafers) no pin-hole has been found.



Fig.2. The distribution of breakdown voltages of coupling capacitor with ONO and SiO².

Gettering Technology: The other consideration (5) for large area sensors is leakage current of microstrip. In order to reduce the leakage current, some gettering process had been developed and tested. The results are listed in Table 1. The condition which used ERSO's CCD gettering technology with backside polysilicon and ONO deposition process was found to be the best one. The gettering process was composed of intrinsic gettering and extrinsic gettering technology. The intrinsic gettering used the ERSO's CCD gettering technology which was modified from 3-step oxidation gettering. After the polysilicon bias resistor and ONO capacitor process, the second gettering process with extrinsic gettering was used. The leakage current of the best 8×4 cm² sample was 2 μ A, this was also the lowest one for the 8×4 cm² sensors reported.

Table 1 The detector leakage of different gettering processes

Condition		B	C	D	E	F	G	Н	1
leakage	800	200	200	1000	800	450	80	500	200
(nA/cm)		1	1	1	1	1	1	1	1
	1200	300	300	1200	1000	700	100	700	300

*100 Volts reversed bias

*A: backside N+ doped

B: backside Polysilicon deposition

C: backside Polysilicon and ONO deposition

D: High temperature gettering E: Condition D with B

F: Low and High temperature gettering

G: ERSO CCD gettering process with condition C

J. EKSO CCD genering |

H: Condition A with F

(C) Implant damage: From the test result of test key, we found the leakage current was function of the distance from the center of wafer. The leakage of test pattern close to the center of wafer was much smaller than that of test pattern near the edge of wafer, shown in Fig. 3. By the study of sirtl etch analysis, the leakage was found to be caused by the implant damage, shown in Fig. 4(a) and (b).Boron solid source diffusion process has been proposed to replace the P+ strip implant process.







Fig. 4: The implant damage found at the (a) test pattern near the edge of wafer (b) the edge of 8×4 cm² sensor.

4. EXPERIMENT RESULTS

(a) Beam test: $8 \times 4 \text{ cm}^2$ and $2 \times 2 \text{ cm}^2$ microstrip sensors had been fabricated.

The $8 \times 4 \text{ cm}^2$ prototype sensors were bonded with SVX chips and tested at CERN in 1993. An average S/N ratio of 30 and an efficiency above 97% were obtained.

From the study reported by Y.H. Chang et. al. (b), the intrinsic resolutions obtained with the corresponding residual of Monte Carlo simulation data are listed in Table 2.

The $8 \times 4 \text{ cm}^2$ sensor - N9, made by this proposed process (by implant not by solid source diffusion), gets the best spatial resolution

of 3.5 \pm 0.5 μ m with efficiency close to 100%.

Table 2 The residuals (um) of Y-senors in linear track fitting

	N4	N9	J1	N3	C1	C2
int.rcs. (um)	6.1	3.5	9.4	5.1	7	10.5
6	4.45	4.22	8.82	6.02	6.71	7.82
5	3.93	4.08	8.35	5.28	5.46	*12.93
5	4.44	4.21	8.63	6.25	*9.72	6.45
5	4.4	4.15	8.94	*7.79	0.72	6.99
5	3.81	3.95	*10.41	6.2	6.58	7.21
5	3.83	*7.07	8.5	5.98	6.82	7.83
5	*9.17	4.04	8.04	6.01	6.69	7.26
4	3.61	3.97	*11.12	*8.32	6.72	6.14

* : detector excluded in the fitting.

(b) Modifure test: Because the process flow had been rearranged, all the active area except the contact holes was covered with the ONO dielectric. As we know, silicon nitride is a good diffusion mask so the sensor could be prevented from moisture.

The frabricated 2×2 cm² sensors had been passed the 85% relative humidity and

85 °C environment test, an IEC standard environment test condition.(7)(8)

A 2×2 cm² single metal sensor stayed in air for one year after the beam test in 1992, the same sensor was used in 1993 for test beam at CERN. It's performance was still good enough and almost the same as last year.

5. CONCLUSION

An improved process with ONO dielectric has been shown to produce 8×4 cm³ silicon microstrip sensors of satisfactory electrical properties. The breakdown voltage of the ONO capacitor is higher than 200V for loop test and 2×2 cm³ sensors, and is higher than 160V for the 8×4 cm³ sensors. It was also pin-hole free process which had a high production yield. Optimum condition - ERSO's CCD intrinsic gettering technology with backside pollysilicon and ONO

deposition extrinsic gettering process for P^+ strip sensor has been found. The major leakage comes from the edge of wafer caused by implant damage, and has been found. The boron solid source diffusion process has been proposed to solve the problem. From the results of beam test at CERN in 1992 and 1993, we found the proposed process had high S/N ratio, efficiency, resolution, and reliability. We have prepared a long ladder prototype which consists of 8 8×4 cm³ sensors to be tested at CERN 1994 summer.

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