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Large Electron Transfer and Strong Negative Differential Resistance in Strained InGaAs Channel Real-Space Transfer Transistors

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Real-space transfer transistors with a $In_{0.15}Ga_{0.85}As$ channel layer are fabricated. These devices show large electron transfer and strong negative differential resistance behaviors. The drain current peak-to-valley ratio can be larger than 3000 at room temperature and more than one million (10^6) at 77 K. The performance improvement is attributed to the formation of source/drain heterojunction in the InGaAs channel device with Pd/Ge ohmic contacts.

1. Introduction

Real-space transfer (RST) transistors have been actively studied since 1979.[1-5] RST devices are based on hot carrier transfer between two conducting layers. For RST transistors made with the GaAs/AlGaAs material system, channel electrons in GaAs layer will be accelerated and become "hot" when a bias voltage is applied between the source and drain terminals. Hot electrons will have sufficient energy and can flow across the AlGaAs potential barrier to reach the collector terminal. This electron transfer results in an increase of collector current and a decrease of drain current. A negative differential resistance (NDR) is therefore obtained in the drain current.

The device performance of RST transistors can be improved by using GaAs/InGaAs/AlGaAs heterostructures on GaAs substrates[6,7] or InGaAs/InAlAs heterostructures on InP substrates.[8,9] Due to the lower electron effective mass (m^*) in the InGaAs material and larger conduction-band discontinuity (ΔE_C) in the InGaAs/AlGaAs or InGaAs/InAlAs heterojunctions, the InGaAs channel RST transistors show larger electron transfer and lower leakage current from the source/drain contact areas to the collector. For RST transistors used in logic or optical applications, large transferred current and low leakage current are two important key parameters that determine the logic/optical on/off ratio.[5,10] Large electron transfer also enhances the NDR effect and gives higher drain current peak-to-valley ratio.

In this work, an InGaAs channel RST transistor is fabricated with GaAs/InGaAs/AlGaAs heterostructures. In order to avoid electrical shorting between the source/drain contacts and the collector layer, Pd/Ge ohmic contact is used instead of the conventional AuGe-Ag-Au contact. Because the Pd/Ge ohmic contact is non-alloyed and very shallow,[11] the source/drain contacts formation is not as critical as that of AuGe-Ag-Au contact which considerably eases the fabrication of RST transistors.[12,13]

2. Experiment

The epitaxial structure of a strained InGaAs channel RST transistor is shown in Fig. 1. The epitaxial heterostructure is grown on a semi-insulating GaAs substrate by molecular beam epitaxy (MBE) using a Varian Gen II machine. The device structure consists of the following layers: a 0.8μm n^+GaAs collector layer (Si: 2×10^{18} cm^{-3}), a 200Å undoped GaAs layer, a 2000 Å undoped $Al_{0.45}Ga_{0.55}As$ barrier layer, a 200Å undoped $In_{0.15}Ga_{0.85}As$ channel layer, a 50Å undoped GaAs layer, and a 250Å n^+GaAs layer (Si: 2×10^{18} cm^{-3}) for top ohmic contacts. After MBE growth, standard photolithographic process is used for

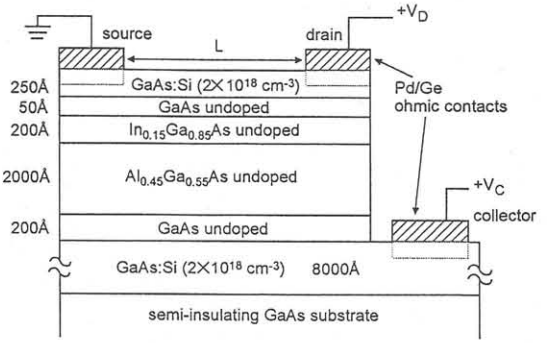

Fig. 1. Schematic diagram of a strained InGaAs channel RST transistor. The source, drain, and collector contacts are all made with Pd/Ge. Channel length L=2 μm.

device fabrication. Pd(500Å) and Ge(1250Å) are then deposited sequen-tially by electron beam evaporation. The Pd/Ge ohmic contacts are formed by rapid thermal annealing at 450°C for 1 minute. The device channel length is 2μm and the width is 150μm.

3. Results

Fig. 2 shows the collector current I_C versus drain voltage V_D with different collector voltages V_C at room temperature (the source terminal is grounded). The measured I_C at V_D=0 V is due to the leakage current from the source/drain contacts to the collector. As V_D increases, I_C decreases initially. This is due to a decrease of collector-to-drain bias which reduces the drain-to-collector leakage current. When V_D is larger than 0.8 V, transferred current into the collector becomes dominant which results in the increase of I_C. In addition, the increase of V_C causes a increase in channel electron concentration and hence induces larger transferred current. However, the increase of V_C also causes an increase of leakage current at. Fig. 3 shows I_C versus V_D with different V_C at 77 K. The leakage current is suppressed at low temperatures. When V_D is large than 0.5 V, the transferred current becomes dominant and I_C increases sharply.

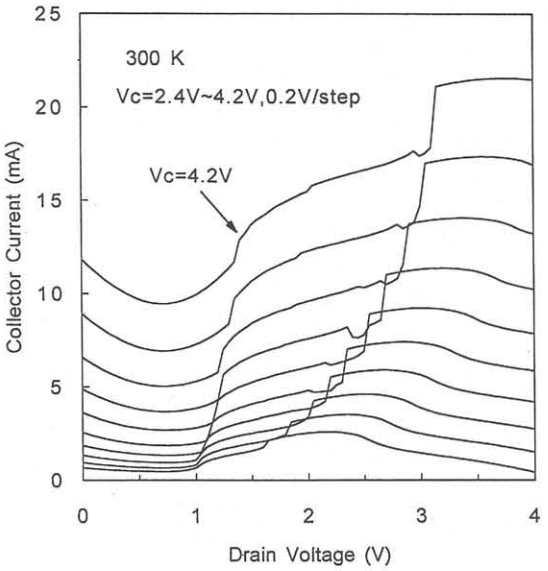

Fig. 2. I_C vs. V_D with different V_C at 300K. V_C increases from 2.4V to 4.2V with 0.2V per step.

When the RST transistors are operated in the negative resistance field-effect transistor (NERFET) mode,[2] they show strong NDR behavior in the drain current. Fig. 4 shows the drain current I_D as a function of V_D for ten different V_C at 300 K. When V_D increases initially, I_D increases also. Different V_C gives different slopes with increasing I_D. This operation is similar to that of a back-gate field-effect transistor. When V_D is about 1V~1.3V, the drain current reaches the highest value and then decreases with a NDR effect. At even higher V_D, the drain-collector bias becomes positive which reduces the electron transfer from

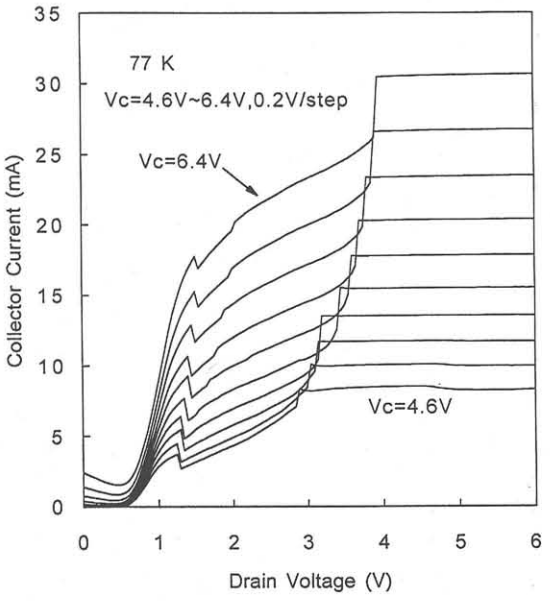

Fig. 3. I_C vs. V_D with different V_C at 77K. V_C increases from 4.6V to 6.4V with 0.2V per step.

channel to the collector and also attracts electrons from the collector to the drain. These lead to an increase of drain current.

The NDR characteristics are improved even further at low temperatures. Fig. 5 shows the I_D characteristics at 77K. The peak drain current occurs at about V_D=1.2~1.5V. When V_D increases further, the I_D shows sudden step-drop features which are sharper than those observed at room temperature. The saturated region of valley current is quite wide and extends from about V_D=3V to V_D=10V. The saturation of I_D is clearly indicated by a current plateau of I_C in Fig. 3. The valley current can be reduced to less than 1μA for V_C>6V.

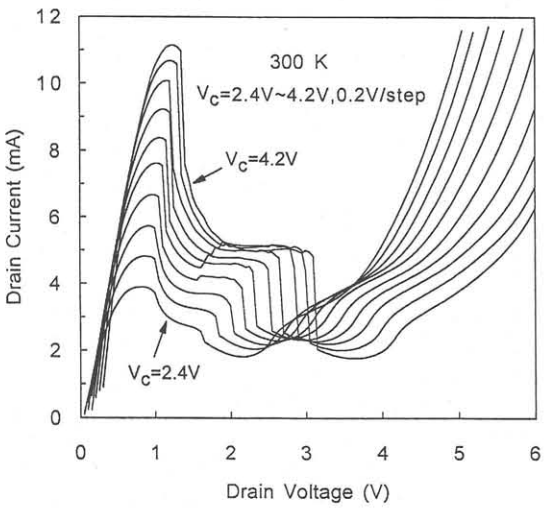

Fig. 4. I_D vs. V_D with different V_C at 300K. V_C increases from 2.4V to 4.2V with 0.2V per step.

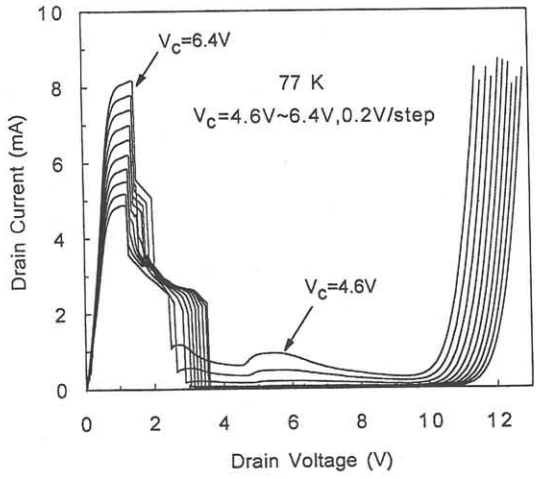

Fig. 5. I_D vs. V_D with different V_C at 77K. V_C increases from 4.6V to 6.4V with 0.2V per step.

The peak-to-valley ratio (PVR) of I_D is an important parameter in NERFET mode operation. At 300K, the highest measured PVR is 3210 at V_C=5V. The average value is 2820. This is the highest PVR obtained for GaAs-based NERFETs measured at 300K.[7,14] At 77K, the PVR becomes very large and can be larger than one million (10^6) for V_C>7.6V. To our knowledge, this is the largest NERFET drain current PVR reported at 77 K. The PVR increases by about six orders of magnitude from 6.5 to 4.9×10^6 when V_C increases from 4V to 8V. This demonstrates that the PVR is controllable in the strained InGaAs channel RST transistors.

4. Discussion

The InGaAs channel RST device shows large transferred current and high drain current PVR. The device performance is improved over those reported previously.[7] This is attributed to the formation of heterojunction source-channel and drain-channel configurations due to the utilization of shallow Pd/Ge ohmic contacts. The Pd/Ge ohmic contacts are very shallow (~150Å)[15,16] so that the source/drain contact depths remain inside the n^+GaAs layer and do not reach the InGaAs channel layer (Fig. 1). The GaAs/InGaAs heterojunctions beneath the source and drain contact areas are still preserved. Therefore, the electrons are injected at the source-channel heterojunction from the GaAs source terminal (larger bandgap material) to the InGaAs channel (smaller bandgap material) with an injection energy about equal to the conduction band discontinuity (ΔE_C). This injection energy will help the electron transfer.[17] In addition, residual low-energy channel electrons can be blocked by the drain-channel heterojunction.[17] This gives lower valley drain current. As a result, a large transferred current and a high PVR is obtained in the strained InGaAs channel RST transistors.

5. Conclusions

Strained InGaAs channel RST transistors are fabricated and good device performance is achieved. These devices show large electron transfer and strong negative differential resistance at room temperature and 77 K. The best peak-to-valley ratio is larger than 3000 at room temperature and more than one million at 77K. The improvement of device performance is attributed to the formation of source-channel and drain-channel heterojunctions with shallow Pd/Ge ohmic contacts.

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