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Invited

A Manufacturable High-Speed Low-Power Complementary GaAs Process

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A self-aligned complementary GaAs heterostructure FET process, has been successfully established for low power, high-speed circuits. The devices are based on AlGaAs/InGaAs/GaAs heterostructures grown by MBE on 4-inch LEC GaAs substrates. The process uses twelve lithographic steps through two levels of interconnect. 0.7 x 10 μm N-channel and P-channel devices typically show transconductances of 300 mS/mm and 70 mS/mm respectively. Twenty three stage unloaded complementary ring oscillators of 0.7 x 10 μm N- and P-FET's show propagation delay of 150 ps and speed x power product of 6.9 fJ or 0.293 μW/MHz.

INTRODUCTION

Complementary GaAs technology will offer significant speed-power advantage over Si CMOS circuitry of equivalent gate dimensions, due to the higher carrier velocities and low voltage operation. We have established a complementary GaAs process (CGaAs^{TM}) in Motorola for low-power, high-speed circuits based on AlGaAs/InGaAs heterostructure insulated gate FET's and evaluated the performance of a number of test circuits including ring oscillators, 4K SRAM, divide-by 127/128 pre-scaler and a 16-bit multiplier accumulator. These demonstrations show CGaAs^{TM} to be promising for single battery (0.9-1.5 V) high performance circuit applications.

CGaAs^{TM} PROCESS

A cross-section of the epitaxial material is shown in Fig. 1.The epitaxial structure consists of 30Å GaAs cap/ 250Å of undoped AlxGa1-x As (x=0.75) / 150Å undoped InyGa1-yAs(y=0.2)/undoped GaAs buffer grown on LEC GaAs substrates. Device threshold voltage is adjusted with a silicon pulse doping provided 30Å below the InGaAs quantum-well channel. Both MBE and MOCVD materials have been utilized, yielding high performance devices and circuits. Details of the process have been described elsewhere [1]. Key features include: refractory TiWN gates with SiN/SiO sidewalls, self-aligned by ion implantation of Si for NFET's and F+/Be for PFET's activated by RTA, oxygen implant isolation, and universal refractory ohmics. The ohmic metallization works for both N-channel and P-channel FET's and is stable to temperatures as high as 600 °C. This high temperature non-gold based ohmic allows us to utilize VLSI aluminum interconnect technology for the two levels, where the AlCu deposition occurs using physical vapor deposition (PVD) at 500°C.

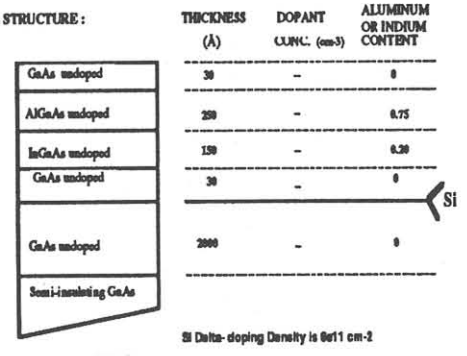

Fig. 1. CGaAs^{TM} Epitaxial cross-section

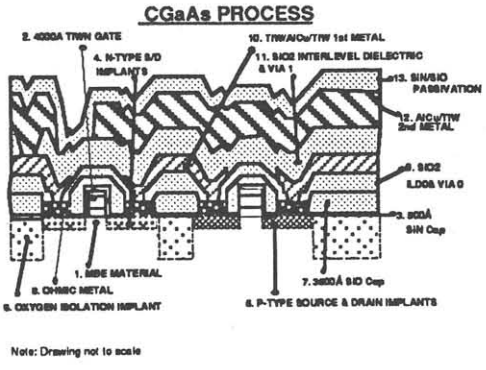

Fig. 2. Schematic cross-section of CGaAs^{TM} process

Figure 2 shows a schematic of the process. The CGaAs process has been designed to be highly synergistic with our GaAs E/D MESFET process in Motorola's Compound semiconductor manufacturing line.

DEVICE RESULTS

Typical 1 x 10 μm N-channel and P-channel FET's show extrinsic transconductance of 250 mS/mm and 60 mS/mm, respectively. Wafer-to-wafer reproducibility of threshold voltage is 70 mV and on wafer standard deviation of Vt is typically 25 mV. Figure 3 shows Vt variation from wafer-to-wafer in several lots with a target NFET Vt of 0.5 V. Devices of target NFET threshold voltage near 0.6 V and P-FET's -0.4 V have also been evaluated. On wafer threshold voltage variation was typically 15 mV, one standard deviation, with some wafers exhibiting one sigma variation as small as 5-10 mV.

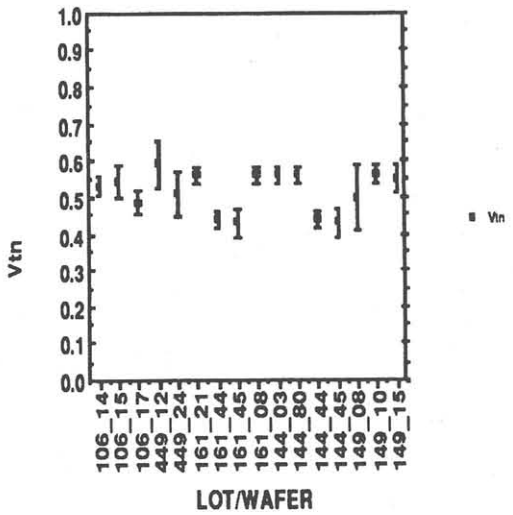

Fig. 3. Wafer-to-wafer and lot-to-lot threshold voltage variation of N-channel FET

The PFET turn-on voltage, defined as the gate voltage resulting in 1 $\mu A/\mu m^2$ gate current at Vds=0 is -2V. The NFET's correspondingly show turn-on voltage of 1.75 V. Subthreshold leakage currents of under 10 nA, as measured at Vgs=0 V and Vds=1.5 V for NFET's or -1.5 V for PFET's, are achieved for 1 x 10 μm N-channel and P-channel devices (Fig. 4). The subthreshold slopes are 75-80 mV/decade for NFET's and 90-100 mV/decade for PFET's. The subthreshold leakage currents of PFET's generally, are very sensitive to decreasing FET gate lengths, due to implant straggle effects, stress enhanced diffusion of the p-type dopant under the gate and drain-induced barrier lowering. The subthreshold currents of submicron PFET devices reported here are the best to our knowledge in complementary GaAs development.

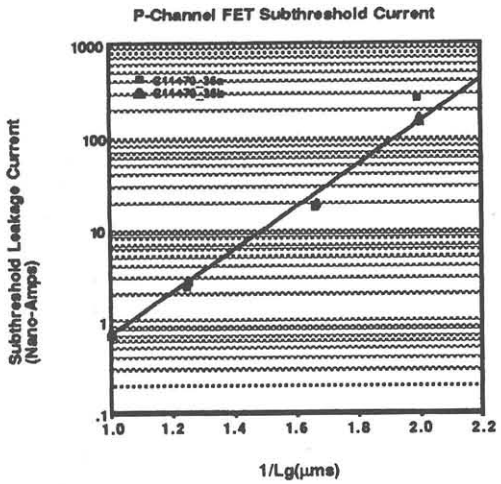

Fig. 4. Subthreshold Leakage currents of PFETs with gate lengths 0.5-μm to 1-μm versus inverse gate length (1/Lg).

RING OSCILLATOR PERFORMANCE

23-stage complementary ring oscillators of various gate lengths were fabricated. Figure 5 shows typical propagation delay as a function of power supply voltage for 10 μm -wide NFET and PFET ring oscillators at FO=1. Propagation delay as low as 150 ps at speed x power product of 6.9 fJ/gate or 0.293 μW/MHz.was achieved. Propagation delay of under 20 ps/gate is also achieved with 0.44-μm gate length devices at a supply voltage of 1 V, showing the promise of this technology for low power applications. The ring oscillator performance is compared to 0.5 μm and 0.8 μm CMOS ring oscillators, indicating the superior performance characteristics of CGaAs™.

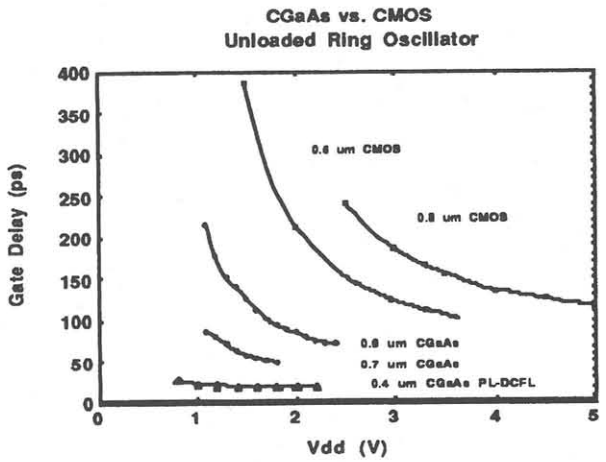

Fig.5. Comparison of 23-stage ring oscillator delay versus supply voltage as a function of gate length for CGaAs circuits with CMOS circuits of gate lengths 0.5 and 0.8-μm. CGaAs shows significant speed advantage.

PRE-SCALER PERFORMANCE

Fully functional divide-by 256/257 pre-scalers were fabricated. The 0.8 x 10 μm pre-scalers operated at 1.01 GHz at a supply voltage of 1.1 V and power dissipation of 377 μW. The CGaAs divide-by 256/257 pre-scaler is compared to that of divide-by 127/128 pre-scalers of several technologies including silicon bipolar, CMOS and GaAs DCFL in Figure 6.

NTT's 0.25-μm SIMOX technology shows the closest power dissipation in the benchmark. For equivalent gate lengths, CGaAs shows more than 3 X speed-power advantage.

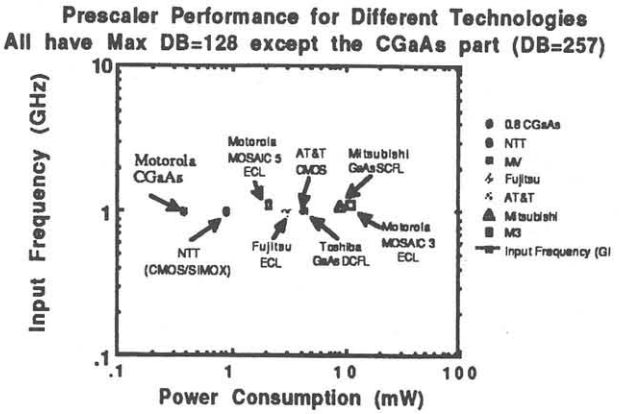

Fig.6. Comparison of CGaAs 256/257 pre-scaler to other pre-scalers

4K SRAM PERFORMANCE

A 4 K SRAM with a 256 x 16 architecture and standard 6T bitcells was designed and fabricated in both 1-μm and 0.7-μm gate CGaAs. The SRAM was derived from a 5 V CMOS DSP56156 design with minimal modification made to allow the CGaAs version to work at 0.9-1.5 V. The SRAM had full complementary logic (no N-channel-only logic in critical paths). The bitcell size was 15.6 μm x 17.8 μm and the size of the SRAM core was 1.14 mm^2. Details of the SRAM design are to be reported elsewhere [2]. Results of access time and power dissipation using 0.7-μm gate length CGaAs devices are compared to SRAM results [3] of Si bipolar, GaAs E/D MESFET, and HBT, and HEMT in Figure 7.

16-BIT MULTIPLY/ACCUMULATOR

A 16-bit modified Booth multiplier with a 3-way 40 bit accumulator was designed and fabricated using 1-μm CGaAs technology. The multiplier, like the 4 K SRAM was a redesign of CMOS multiplier accumulator in DSP56156. The multiplier used 11,200 transistors in area of 1.22 mm^2. The same circuit in CMOS was 13% larger in area. At 0.9 V, the multiplier delay was 44.7 ns and power dissipation 1.8 mW. The fastest delay was 14.2 ns at 1.5 V compared to 33 ns for the 1-μm CMOS part at 5.0 V. Yields greater than 90% were realized for the CGaAs multiplier circuit.

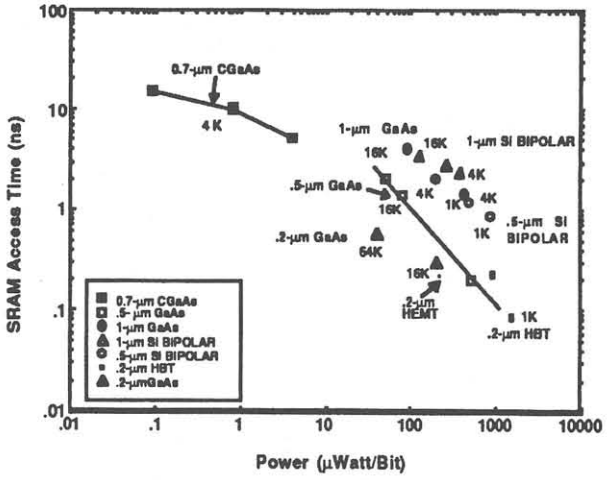

Fig. 7. Comparison of CGaAs™ SRAM speed-power performance to various technologies.

ACKNOWLEDGMENTS

CGaAs™ is a Motorola Trademark

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