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# A New Planar TMT Suitable for L-Band MMICs with RF Transmission and Reception Blocks Operating at Vdd ≦ 2 V

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A new planar-type two-mode channel FET (P-TMT) for L-band MMICs with RF transmission and reception blocks operating at a very low supplied voltage ($V_{dd}$ ≦ 2 V) for use in 1.9 GHz band personal handy phone system (PHS) has been developed. By simply changing the gate width ($W_g$), the P-TMTs were fabricated for both low-noise and high-power applications. At drain voltage ($V_{ds}$)=2 V, a minimum noise figure ($F_{min}$) of 0.65 dB, an associated gain (Ga) of 17.6dB at drain current ($I_{ds}$)=3 mA, and a 1dB gain compression ($P_{o(1dB)}$) of 22.8 dBm at $I_{ds}$=300 mA were obtained. Moreover, at the lower $V_{ds}$=1.5 V, a $F_{min}$ of 0.65 dB, a Ga of 16.9dB at $I_{ds}$=3 mA, and a $P_{o(1dB)}$ of 20.9 dBm at $I_{ds}$=350 mA were obtained.

## Ⅰ. Introduction

In order to achieve greater reductions in size, weight and power dissipation for hand-held wireless personal communication systems such as the personal handy phone system (PHS) using π/4 shift QPSK (Quaternary Phase Shift Keying), transmission amplifiers and reception amplifiers with low power dissipation and low voltage operation must be developed. The low voltage operation enables a reduction in battery size and the low power dissipation in whole the system resulting in long-time operation.

It was reported that a GaAs power MESFET [1] for the transmission amplifier offers high efficiency in low voltage operation, and that a GaAs JFET [2], GaAs MESFET [3] and HEMT [4] for the reception amplifier provides good low-noise performance with low power consumption. However, these devices must be fabricated on different wafers or on the same wafer using a different wafer process. There have been no reports on both low-noise and high-power devices , which operate in either a low voltage or low power condition, being fabricated on the same wafer using the same wafer process for a single-chip MMIC to unify transmission and reception MMICs.

We have developed a super-low-noise two-mode channel FET (TMT) [5] with high- and plateau-shaped transconductance characteristics for low-noise and high-power applications, which has high potential for realizing a single-chip MMIC to unify transmission and reception MMICs.

A new planar-type TMT(P-TMT) for L-band MMICs with RF transmission and reception blocks operating at a very low supplied voltage ($V_{dd}$ ≦ 2 V) for use in 1.9 GHz band PHS has been successfully developed. Both low-noise and high-power P-TMTs can be fabricated on the the same wafer using the same wafer process by simply changing the gate-width ($W_g$) so that provide a simple wafer fabrication process and reduce the fabrication cost.

In this paper, we report on the P-TMT structure, fabrication process and DC characteristics. Next, the low-noise and high-power characteristics obtained by simply changing the $W_g$ are shown.

## Ⅱ. Device Structure

Figure 1 shows the device structure for the P-TMT, which is designed for common use in both low-noise and high-power applications. The wafer consists of an undoped GaAs buffer layer, an undoped InGaAs channel layer (In mole fraction 0.2, 50 Å), an undoped graded $In_xGa_{1-x}As$ channel layer (In mole fraction 0.2(lower side)～0(upper side), 70 Å), an undoped GaAs spacer layer (75 Å), an n-GaAs electron-supplying and channel layer ($n=2.5\times10^{18}$ $cm^{-3}$, 200 Å), an n-AlGaAs barrier layer, an undoped AlGaAs barrier layer and an undooped GaAs barrier layer. The wafer was grown by the molecular beam epitaxy (MBE) method at a GaAs substrate temperature of about 500 ℃. The unique points of the structure include

the introduction of an undoped AlGaAs/GaAs barrier layer to achieve a high breakdown voltage ($V_B$) and an $n^+$ self-aligned-gate implantation process using a single-layered dummy-gate to realize a low source series resistance ($R_s$), in which SiN double-layered films prepared by ECR-plasma-CVD were used as annealing encapsulants so as to gain a high activation efficiency in Si implanted regions [6].

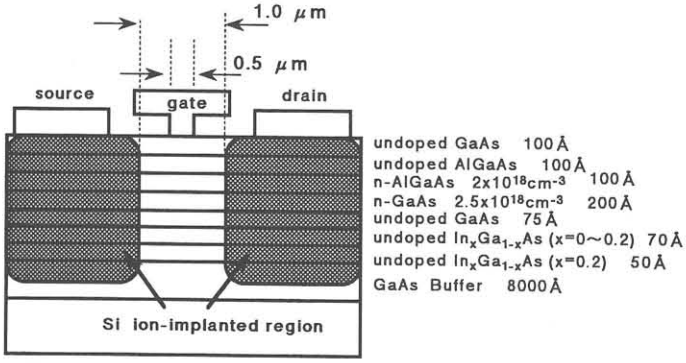


Fig. 1. Schematic cross section of planar-type TMT structure.

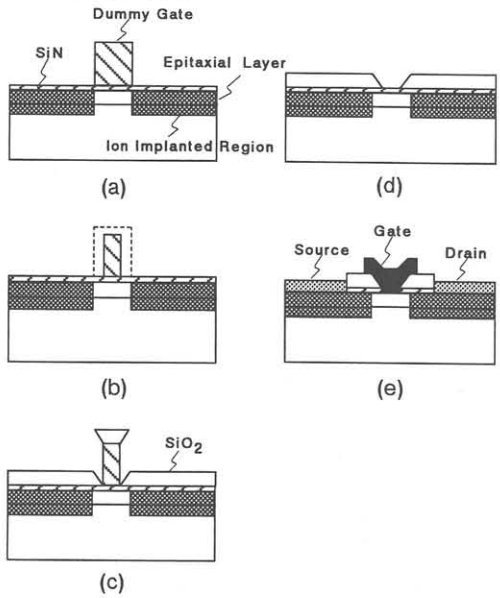


Fig. 2. Device fabrication process of P-TMT

## Ⅲ. Device Fabrication Process

The device fabrication process for our improved $n^+$ self-aligned P-TMT is shown in Fig. 2. After device isolation through mesa etching, a SiN anneal cap was deposited by ECR-plasma-CVD. Next, an optically exposed 1.0 $\mu$m-length dummy-gate pattern was shaped using a PMMA photoresist (Fig. 2(a)). Then, self-aligned $n^+$ regions (100 KeV, Si dose $4\times10^{13}$ $cm^{-2}$) were formed by Si implantion using the dummy-gate pattern. The dummy-gate pattern was thinned from 1.0 $\mu$m to 0.5$\mu$m by oxygen plasma (Fig. 2(b)). After $SiO_2$ deposition using the ECR-plasma-CVD method followed by selective wet etching (buffered HF) of the $SiO_2$ deposited on the sidewall of the dummy-gate resist (Fig. 2(c)), the reverse dummy-gate pattern was formed by removing the resist followed by rapid thermal annealing (Fig. 2(d)). Alloyed AuGe/Ni/Au metal was used for the source and drain ohmic contacts. The T-shaped gate electrode was fabricated by a lift-off of the evaporated Ti/Pd/Au metal (Fig. 2(e)). Finally, after depositing the SiN passivation film, a source bridge electrode was formed using polyimide films. The gate length and width were 0.5 and 400 $\mu$m (100 $\mu$m×4 gate fingers) for the low-noise TMT, and 0.5 and 2600 $\mu$m (100 $\mu$m×26 gate fingers) for the high power TMT, respectively. The rapid thermal annealing condition of 880℃ for 5 seconds was used in order to obtain a higher electron concentration especially in the surface region, which was the optimum activation condition for the low acceleration energy (15 KeV) ion-implanted region as shown in Fig. 3.

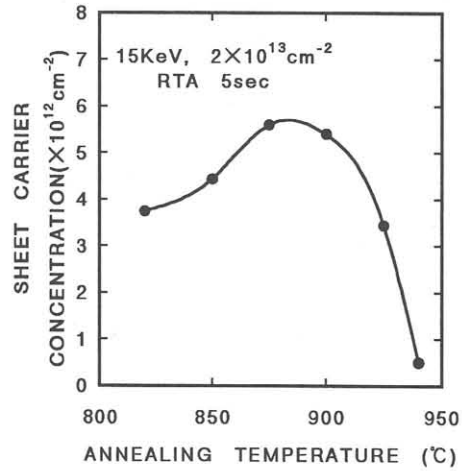


Fig. 3. Sheet carrier concentration as a function of annealing temperature.

## Ⅳ. Device Characteristics

Figure 4 shows the transconductance ($g_m$) and the drain current ($I_{ds}$) as a function of the gate voltage ($V_{gs}$) for the 0.5 $\mu$m P-TMT. The 0.5 $\mu$m P-TMT has a plateau-shaped, high $g_m$ with about 200 mS/mm at the relatively wide $V_{gs}$ region of -0.6 ~+0.4 V corresponding to the high Ids region of 82~280 mA/mm, and a high $g_m$ of more than 85 mS/mm even at the very low $I_{ds}$ of 7.5 mA/mm. A high $V_B$ of more than 8V and a low $R_s$ of less than 0.6 Ω · mm were obtained.

Figure 5 shows the minimum noise figure ($F_{min}$) and associated gain (Ga) as a function of the frequency in low power operation at $V_{ds}$=2 V, $I_{ds}$=3 mA for the low-noise P-TMT ($W_g$= 400 $\mu$m). The $F_{min}$ of 0.65 dB and the Ga of 17.6 dB were

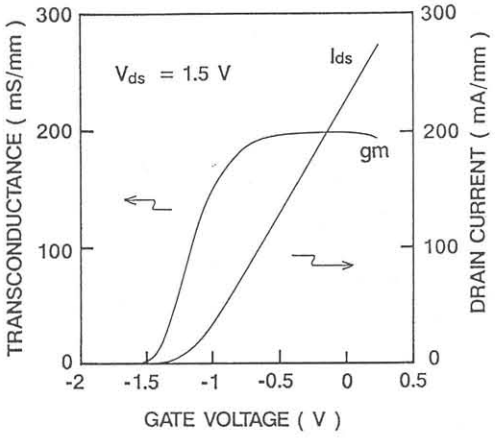


Fig. 4. Transconductance and drain current as a function of gate voltage.

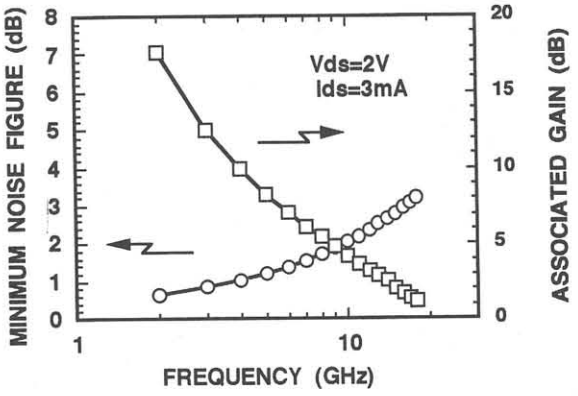


Fig. 5. Minimum noise figure and associated gain as a function of frequency at $V_{ds}$=2 V ($W_g$= 400 $\mu$m).

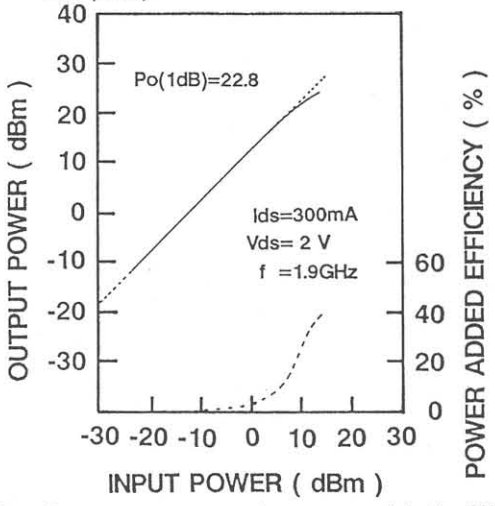


Fig. 6. Output power and power-added efficiency as a function of input power at $V_{ds}$=2 V and 1.9 GHz ($W_g$= 2600 $\mu$m).

obtained at 2 GHz. At $V_{ds}$=1.5 V, $I_{ds}$=3 mA, the $F_{min}$ of 0.65 dB and the Ga of 16.9 dB were obtained at 2 GHz. At $V_{ds}$=1.2 V, $I_{ds}$=3 mA, the $F_{min}$ of 0.65 dB and the Ga of 15.1 dB were obtained at 2 GHz.

Figure 6 shows the output power and power-added efficiency as a function of the input power for the high-power P-TMT ($W_g$= 2600 $\mu$m) measured at a $V_{ds}$ of 2 V at 1.9 GHz. An output power (1 dB gain compresssion $P_{o(1dB)}$) of 22.8 dBm, a power-added efficiency ($\eta_{add}$) of 32.3 % and a 3rd order intercept point ($IP_3$) of 35.3 dBm at $I_{ds}$=300 mA were obtained. At a $V_{ds}$ of 2 V and $I_{ds}$=240 mA, a $P_{o(1dB)}$ of 22.1 dBm and a power-added efficiency $\eta_{add}$ of 34.4 % were obtained. This output performance is sufficient for PHS use. Moreover, at a lower $V_{ds}$=1.5 V, a $P_{o(1dB)}$ of 20.9 dBm, a $\eta_{add}$ of 23.1 % at $I_{ds}$=350 mA were achieved. At a $V_{ds}$ of 1.5 V and $I_{ds}$=300 mA, a $P_{o(1dB)}$ of 20.6 dBm and a $\eta_{add}$ of 25.0 % were obtained.

## V. Conclusions

A new planar-type two-mode channel FET (P-TMT) for L-band MMICs with RF transmission and reception blocks operating at a very low $V_{dd} \leqq 2$ V for use in 1.9 GHz band PHS has been successfully developed. Using the same fabrication process and simply changing the $W_g$ on the single wafer, P-TMTs with $W_g$= 400 $\mu$m and $W_g$=2600 $\mu$m were fabricated for low-noise and high-power applications, respectively. At a $V_{ds}$=2 V, a $F_{min}$ of 0.65 dB, a Ga of 17.6dB at $I_{ds}$=3 mA, and a $P_{o(1dB)}$ of 22.8 dBm at $I_{ds}$=300 mA were obtained. Moreover, at a lower $V_{ds}$=1.5 V, a $F_{min}$ of 0.65 dB, a Ga of 16.9dB at $I_{ds}$=3 mA, and a $P_{o(1dB)}$ of 20.9 dBm at $I_{ds}$=350 mA were obtained. These results indicate that the newly developed P-TMT is one of the best active device structures available for a single-chip MMIC unifying L-band transmission and reception MMICs in terms of providing a simple wafer fabrication process as well as the excellent performance described above.

## References

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