Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 598-600



# A Buried-Channel $WN_x$/W Self-Aligned GaAs MESFET Process with Selectively-Implanted Channel and Undoped Epitaxial Surface Layers for MMIC Applications

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The combined process of epitaxy and ion-implantation has been developed in a buried-channel WNx/W self-aligned GaAs MESFET. The MESFET comprises an ion-implanted channel layer and an undoped surface epitaxial layer. The ion implantation technique leads to IC-oriented process and the epitaxial technique to buried channel structure. Both an easy isolation and an enhanced breakdown voltage were attained, promizing MMICs for L-band digital mobile communication systems.

## INTRODUCTION

The field of mobile communications has been widely expanded to L-band digital mobile radio systems for personal handy phone sets, where GaAs FETs in MMICs with cost-competitive production are strongly demanded.[1,2] GaAs FETs have been fabricated using two processes: an ion-implantation process and an epitaxial process. Each of these processes has some advantages as follows; an ion-implantation process is production-orientated, easy to control the threshold voltage, and easy to achieve electrical isolation among FETs in a planar MMIC chip, while an epitaxial process can realize complicate channel structure, such as found in HEMTs or other devices. However, each process has been used by itself for fabricating GaAs FETs.

This paper describes a buried-channel[3,4] self-aligned MESFET (BC-MESFET) process which consists of the combination of an ion-implantation technique and an epitaxial technique. The ion-implantation process promises IC-orientated FETs and the epitaxial process realizes a buried channel structure. This new MESFET has attained not only an easy isolation but also an enhanced breakdown voltage, which is important characteristics for the reliability of power amplifier operation.

## DEVICE STRUCTURE AND FABRICATION

Figure 1 shows a schematic cross-sectional view of the BC-MESFET together with a conventional asymmetric-type MESFET.[5] The BC-MESFET has a planar structure which is suitable for monolithic ICs. To improve the gate-drain breakdown voltage, semi-insulating undoped i-GaAs epitaxial layer was incorporated between refractory WNx/W gate electrode and Si-implanted n-type channel. The thickness of i-GaAs layer was varied from 2.5 nm to 10 nm to investigate the effect on the breakdown voltage.

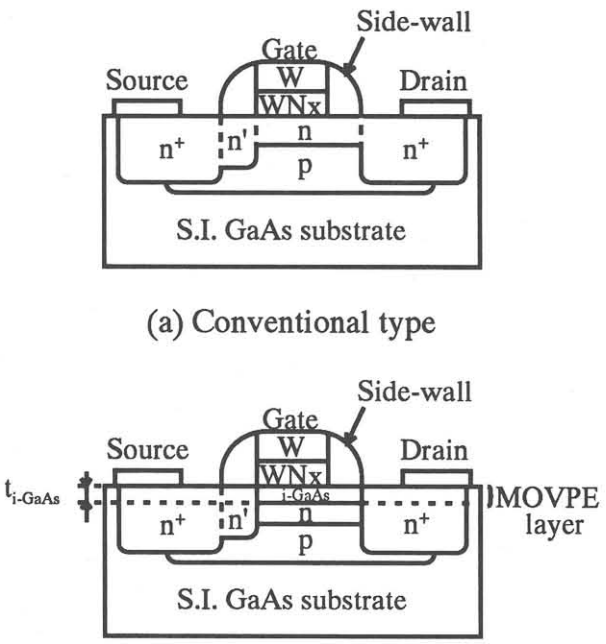


Fig.1. Schematic cross-sectional view of (a) conventional self-aligned MESFET and (b) buried channel MESFET.

An n-type channel region and p-type buffer region were formed by selective implantation of $Si^+$ at 25 keV and $Mg^+$ at 180 keV respectively, before undoped i-GaAs surface layers were grown by MOVPE. Following the deposition and the pattern-etching of WNx/W gate, self-aligned source/drain $n^+$-regions and lightly doped $n^-$-region were also formed by $Si^+$-implantation technique. In order to activate these implanted regions electrically, furnace annealing was carried out at 820℃ for 20 min in a mixed gas of $AsH_3$ and Ar without any encapsulating films. The annealing conditions were decided to achieve maximum activation efficiency of the ion-implanted Si. In this process, the thermal stability of the interface between the ion-implanted layer and the epitaxial layer should be considered from the viewpoint of dopant distributions. Figure 2 shows Si atoms concentration depth-profile by Secondary Ion Mass Spectroscopy (SIMS) measurement. The accumulation of Si atoms are observed at the interface. This should be ascribed to the presence of implantation-induced defects at the interface. Therefore, before the growth of i-GaAs epitaxial layers, an extra annealing on the same conditions as described above was carried out to remove these defects.

Other fabrication processes were performed by those of our standard MESFET.[5,6] The gate length and spacing between drain region and gate edge were 0.6 μm and 0.25 μm, respectively.

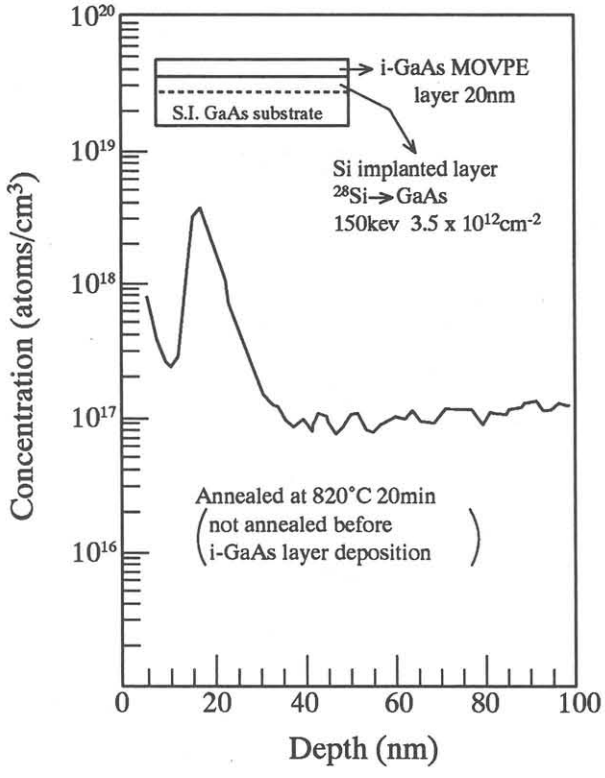


Fig.2. Distribution of Si atoms after annealing.

## DC- AND RF-CHARACTERISTICS

Figure 3 shows a leakage current through a semi-insulating substrate with the annealed 20-nm-thick i-GaAs layer on it, as a function of applied voltage between isolated n-type regions. The leakage current is almost the same as that through a semi-insulating substrate without i-GaAs layer, implying that isolation among FETs is attained for fabricating MMICs.

Figure 4 shows gate-drain and gate-source breakdown voltages of the BC-MESFETs with conventional MESFETs, as a function of threshold voltage. The gate width $W_g$ is 20 μm. Both the breakdown

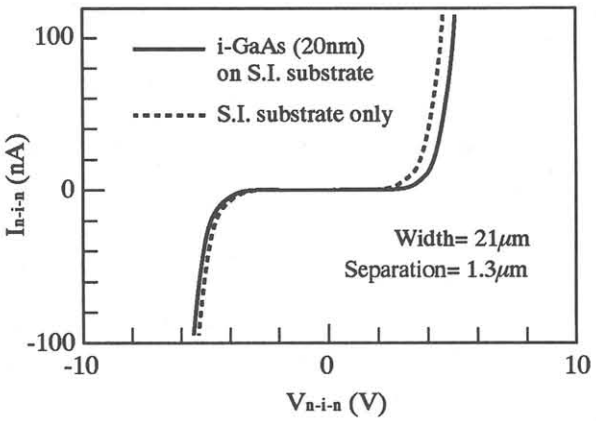


Fig.3. Leakage current $I_{n-i-n}$ of n-i-n structure as a function of applied voltage $V_{n-i-n}$.

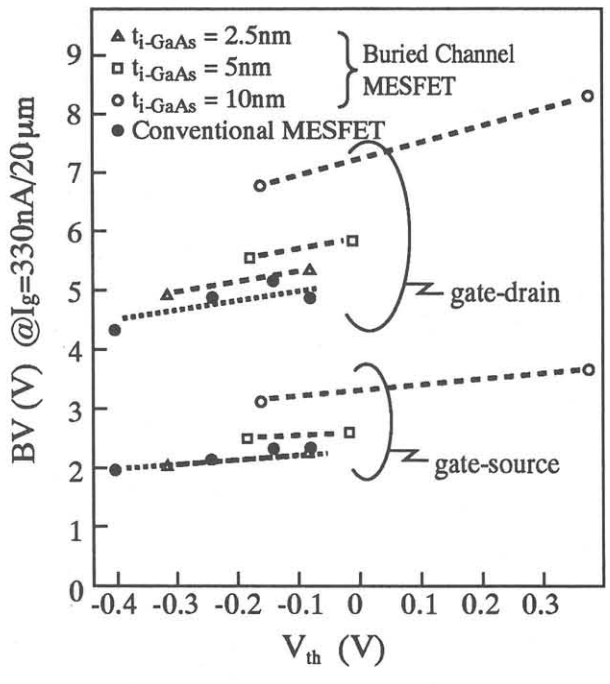


Fig.4. Threshold voltage $V_{th}$ versus breakdown voltage BV for various implantation dosage.

voltages increases with increasing i-GaAs layer thickness, because the highly doped implanted channel is spaced from the gate electrode by semi-insulating i-GaAs layer. A gate-drain breakdown voltage (defined at 330 nA / 20 μm gate current) of 7 V was obtained for the BC-MESFET with 10-nm-thick i-GaAs layer. This value is 2 V higher than conventional MESFETs. The schottky barrier height also increases, and this is mainly attributed to lower channel doping to adjust the threshold voltage.

Figure 5 shows drain current $I_{ds}$ and transconductance $g_m$ of the power BC-MESFET with 10-nm-thick i-GaAs layer as a function of gate voltage $V_{gs}$. This power BC-MESFET is composed of 10 gate-fingers to form 1-mm total gate width. A transconductance of 200 mS at a gate voltage of 0 V and maximum transconductance of 300 mS were obtained, which realize sufficient RF output power performance even at a gate voltage of 0 V. Furthermore, the gate-voltage dependence shows rather broad plateau to provide a better linearity in the RF output power performance. By optimizing i-GaAs layer thickness, it should be possible to improve total performance.

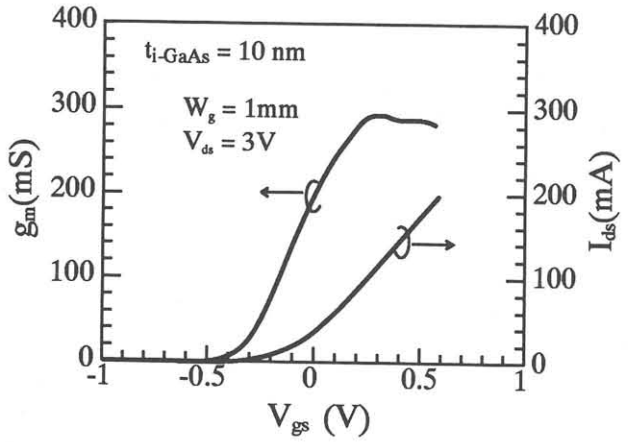


Fig.5. Typical drain current $I_{ds}$ and transconductance $g_m$ versus gate voltage $V_{gs}$.

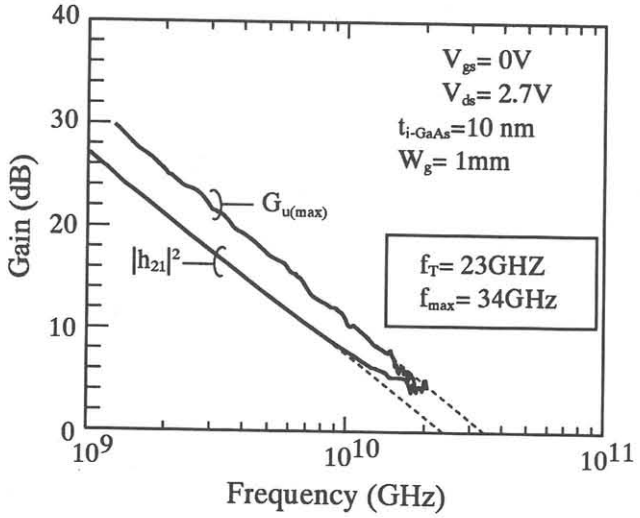


Fig.6. Square of current gain $|h_{21}|^2$ and maximum unilateral gain $G_{u(max)}$ versus frequency.

Figure 6 shows current gain $|h_{21}|$ and maximum unilateral gain $G_{u(max)}$ of the power BC-MESFET with 10-nm-thick i-GaAs layer. These values were calculated from S-parameters at a gate voltage $V_{gs}$ of 0 V and a drain voltage $V_{ds}$ of 2.7 V. A transition frequency $f_T$ of 23 GHz and maximum oscillation frequency $f_{max}$ of 34 GHz were obtained, which are sufficient for L-band power amplification.

## CONCLUSION

The improved gate-drain breakdown voltage has been demonstrated for buried-channel self-aligned gate GaAs MESFETs which comprise ion-implanted channel and i-GaAs epitaxial surface layer. The fabrication is simple and IC-orientated. This FET will be one of the most promising candidates to realize L-band MMICs for use in next-generation digital mobile communication systems.

## ACKNOWLEDGMENTS

The authors wish to thank Dr. T. Arikado and Dr. N. Toyoda. They would also like to thank T. Matsunaga, K. Ishida, A. Kameyama, and S. Obayashi for their various technical contributions.

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