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New Spectroscopic Method for Determination of Energy Distribution of Interface States for MOS Devices with Ultra-Thin Oxide Layers

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XPS measurements are performed under biases for ⟨30Å-Pt/25 Å-silicon oxide/n-Si(100)⟩ and ⟨30Å-Pt/25 Å-oxide/p-InP(100)⟩ MOS devices. The binding energies of the Si($2p_{3/2}$) and In($3d_{5/2}$) peaks with respect to that of the Pt($4f_{7/2}$) peak are shifted by applying biases, and it is attributed to the accumulation of electric charges in interface states. By analyzing the amount of the shifts measured as a function of the bias voltage, the energy distribution of the interface states is obtained.

1. INTRODUCTION

The energy distribution of interface states for MOS devices with thick oxide layers is usually estimated from measurements of electrical characteristics such as capacitance-voltage (C-V)[1] and conductance-voltage (G-V)[2] curves. However, the MOS devices with oxide layers thin enough for electrons to tunnel, such electrical measurements cannot be applied. Moreover, the estimation of the energy distribution of the interface states from the electrical characteristics requires many assumptions such as an equivalent circuit, a uniform dopant density, a smooth interface, etc.

In the present study, a new method to determine the energy distribution of the interface states for MOS devices with extremely thin oxide layers has been developed, based on measurements of X-ray photoelectron spectra (XPS) under biases, which requires no such assumptions as those mentioned above.

2. THEORETICAL BASIS

The MOS devices formed in the present study possess ca. 30 Å-thick Pt and 25 Å-thick oxide overlayers on the semiconductor substrates. The intensity of photoelectrons emitted from the semiconductor substrates is attenuated exponentially with the thickness of the overlayers. Considering that the mean free path of photoelectrons with the kinetic energy of 1 ~ 1.4 keV is in the range between 15 and 25 Å,[3] the signal from the semiconductor substrate is decreased by a factor of ca. 1/20 by these overlayers, but still detectable. The Pt layer 30 Å-thick is almost continuous, resulting in the sufficiently low resistance. Therefore, the XPS spectra for the semiconductor substrate are measurable under biases.

Hereafter, we take an n-type semiconductor-based MOS device under a forward biases as an example. The same argument also holds for a p-type semiconductor and/or for a reverse bias, by changing the signs of the equations appropriately.

Under a zero bias (Fig. 1a), interface states present below the Fermi level, E_F^0, are occupied by electrons, whereas those above E_F^0 are empty. By applying a forward bias (Fig. 1b), the semiconductor quasi-Fermi level, E_F^f, is elevated, and consequently, the

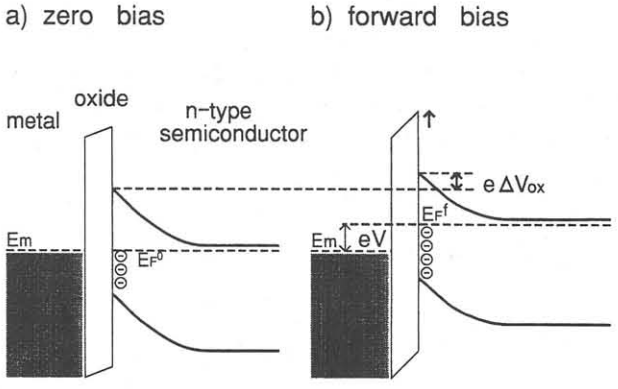

Fig. 1 Band diagrams for an n-type semiconductor-based MOS device: a) at zero bias; b) under a forward bias.

interface states present between E_F^0 and E_F^t are newly occupied by electrons. This increase in the negative charge in the interface states, ΔQ_{ss}, is given by

$$\Delta Q_{ss} = e\int_{E_F^0}^{E_F^t} N_{ss}dE \qquad (1)$$

where N_{ss} is the density of the interface states, E is the energy in the semiconductor band-gap, and E, E_F^0 and E_F^t are defined with respect to the valence band maximum (VBM). This charge, ΔQ_{ss}, causes a change in the potential drop across the oxide layer, ΔV_{ox}, with the magnitude given by

$$\Delta V_{ox} = e\int_{E_F^0}^{E_F^t} N_{ss}(E)dE/C_{ox} \qquad (2)$$

where C_{ox} is the capacitance of the oxide layer. The semiconductor band-edge is fixed with respect to the oxide band-edge, and hence, ΔV_{ox} causes an upward shift of the semiconductor band-edge. The energy between the core level and the band-edge is constant, ΔV_{ox} causes a shift of the core level, which is detectable by means of XPS.

On the other hand, E_F^t is written as

$$E_F^t = E_F^0 - eV - e\Delta V_{ox} \qquad (3)$$

where V is defined to be negative in sign for a forward bias and ΔV_{ox} is positive in sign for an upward band-edge shift. Using eqns. (2) and (3), N_{ss} can be estimated from ΔV_{ox} measured as a function of V.

ΔV_{ox} is also caused by the change in the depletion layer charge. However, for the present devices,it is estimated to be less than scores of ten millivolts, and thus neglected in the present analysis.

3. EXPERIMENTAL

MOS devices were produced from phosphorus-doped n-type Si(100) and Zn-doped p-type InP(100) wafers. After the chemical etching, a ca. 25 Å-thick silicon oxide layer was formed on the Si(100) wafers by keeping the wafers in a humidified air for ca. 24 h. On the InP(100) wafers, a ca. 25 Å-thick oxide layer was formed by immersing the wafers in a mixed solution of $K_2Cr_2O_7$: 50% H_2PO_3 : 47% $HBrO_4$ = 1 : 2 : 2 and keeping them in humidified air for ca. 20 h. On these oxide surfaces, ca. 30 Å-thick Pt layers were deposited by an electron beam evaporation method. After achieving ohmic contact at the rear semiconductor surfaces, the specimens were attached to a copper plate and a lead wire was attached to the front Pt layer with silver paste. The MOS devices thus produced were mounted on a sample plate and inserted into an ultra-high vacuum XPS chamber.

XPS spectra were measured with a PHI 5500 spectrometer. Monochromatic X-ray was irradiated from the Pt layer side at the incident angle of 45°. The front Pt layer was grounded, and the sample plate which was in contact electrically with the rear semiconductor surface was connected to a potentiostat for applying biases.

4. RESULTS AND DISCUSSION

For the n-Si-based MOS devices, the substrate Si($2p_{3/2}$) peak with respect to that of the Pt($4f_{7/2}$) peak is shifted toward the lower (or higher) binding energy by applying forward (or reverse) biases, as shown in Fig. 2a. On the other hand, for the p-InP-based MOS devices, the substrate In($3d_{5/2}$) peak shows shifts toward the higher (or lower) binding energy by applying forward (or reverse) biases, as shown in Fig. 2b. These shifts were completely reversible for the repeated biases, in contrast to usual chemical shifts. The direction of the shifts agrees with that expected from the change in the potential drop across the oxide layer caused by accumulation of electric charges in the interface states.

The energy distribution of the interface states, N_{ss}, is obtained from the analysis of Fig. 2 using eqns. (2) and (3), and the results are shown in Fig. 3. C_{ox} and E_F^0 were obtained from the C-V measurements and the measurements of the temperature-dependence of the current-voltage curves, respectively.

For the Si-based devices, the N_{ss} is high

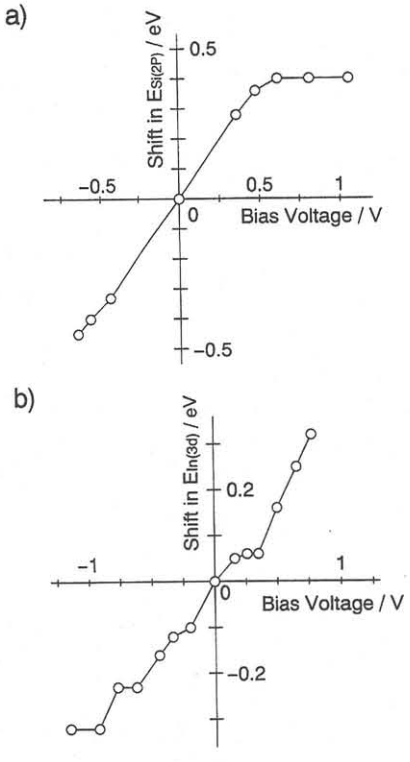

Fig. 2 Amounts of the shift of the Si($2p_{3/2}$) peak (Fig. 2a) and the In($3d_{5/2}$) peak (Fig. 2b) as a function of the bias-voltage.

near the mid-gap. Calculations[4] show that the specific defects such as Si dangling bonds, Si-O broken bonds, oxygen vacancies, Si-Si weak bonds, etc. possess discrete energy levels in the Si band-gap. The N_{ss} observed in the present study has high densities in the relatively wide energy region, probably because several kinds of such defects contribute to the density of states.

For the InP-based devices, the N_{ss} is high in three energy regions, i.e., near the mid-gap, near the VBM, and near the conduction band minimum (CBM). For the metal-deposited Ⅲ-Ⅴ group semiconductors, many models for the Fermi level pinning are proposed. Spicer et al.[5] proposed the unified defect model based on synchrotron UPS measurements. In this model, the semiconductor Fermi level is assumed to be pinned at a discrete energy level of an extrinsic defect state such as vacancies and antisite defects. It is the most probable that the interface states near the mid-gap is due to the occupied phosphorus antisite defects, i.e., P on the In site, because this energy level is calculated to be 0.65 eV above VBM.[6] For another model, i.e., the disorder-induced gap state model,[7] the interface states are suggested to possess U-shaped energy distribution. It is not clear whether the interface states near VBM and CBM are due to the defect states or the disorder-induced gap states.

Finally, the present study is compared with the work done by Lau and Wu.[8] They performed XPS measurements for 20 ~ 30 Å-thick silicon oxide-covered Si surfaces to obtain the energy distribution of interface states. The surface potential is controlled by the charge-up effects, i.e., irradiation of low energy electrons or spontaneous positive charging due to photoemission. In the estimation of N_{ss}, they used the conventional MOS theory in which the counter charge of the surface state charge and the depletion layer charge is assumed to be induced at the surface of the oxide layer (or oxide/metal interface). However, in the absence of a metal overlayer, it is not clear wether all the incident electrons stay at the surface of the oxide layer, not in its bulk. Therefore, it is likely that this assumption leads to a serious error. For the present diodes with the Pt overlayer, the counter charge of the interface state charge is obviously induced at the Pt/oxide interface, and hence, the N_{ss} can be estimated by measuring the change in the potential drop across the oxide layer. Moreover, the surface potential is likely to be changed with time by the charge-up effect, which may also lead to a serious error. It is also thought that the positive charging by photoemission was very difficult to control. In addition, the surface potential was estimated from the C(1s) peak of contaminant carbon which was likely to be present not only at the oxide surface but also in its bulk, leading to an error.

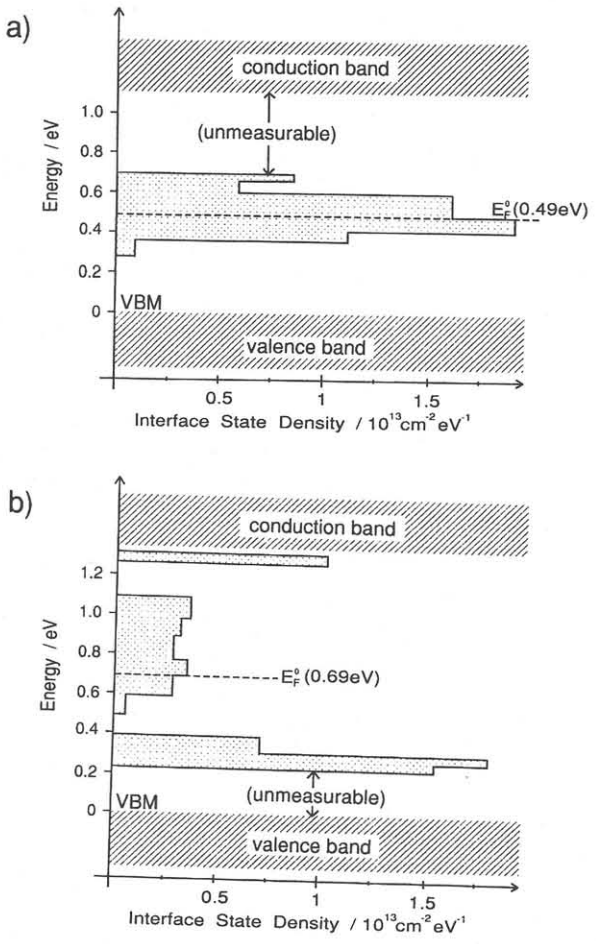

Fig. 3 The energy distribution of the interface states in the band-gap: a) for the ⟨30 Å-Pt/25 Å-silicon oxide/n-Si(100)⟩ device; b) for the ⟨30 Å-Pt/25 Å-oxide/p-InP(100)⟩ device.

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