

Invited

Device-Quality SiO₂/Si(100) and SiO₂/Si(111) Interfaces Formed by Plasma-Assisted Oxidation and Deposition Processes

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We discuss a two-step plasma-assisted process that separates interface formation from film deposition. SiO₂/Si(100) interfaces with a trap density, D_{it} , in the low 10^{10} cm⁻². eV⁻¹ range can be reproducibly formed by this 300°C process. We have applied the process to H-terminated Si(111) surfaces that were made atomically flat by an NH₄F treatment. It is demonstrated that the SiO₂/Si(111) interface prepared in this way has a D_{it} value as low as that for SiO₂/Si(100). We have also found that surface steps that are introduced by intentionally miscutting the (111) surfaces make only minor additional contributions to the D_{it} values.

1. Introduction

Formation of gate-quality SiO₂ at low temperatures is attracting increasing attention because of its potential applications[1-4], not only as a possible alternative to thermally-grown gate oxides, but also as one of the key materials components needed to realize complex and/or novel structures such as compound-semiconductor MOSFET's and three-dimensional devices. The performance and reliability of TFT's also rely on the integrity of vapor-deposited insulators, and their interfaces with poly- or a-Si. Having these potential future applications in mind, we have been studying interfaces between SiO₂ and crystalline Si, as formed by low-temperature plasma-assisted processing. Understanding the physics and chemistry of interface formation on crystalline Si surfaces is a milestone toward the success of other applications requiring low-temperature oxides.

This paper discusses device-quality SiO₂/Si(100) and SiO₂/Si(111) interfaces formed by plasma-assisted oxidation and deposition processes at 300°C[2,5]. We have shown that a two-step process that separates interface formation from film deposition produces SiO₂/Si(100) interfaces with a trap density, D_{it} , in the low 10^{10} cm⁻².eV⁻¹ range. We have applied this two-step process to H-terminated atomically-flat Si(111) surfaces prepared by an NH₄F treatment. These surfaces were characterized by techniques such as AES, LEED, SIMS and spectroscopic ellipsometry (SE)[5,6]. It was shown that SiO₂/Si(111) interfaces prepared in this way had D_{it} values as low as that for SiO₂/Si(100). This observation requires a reexamining of the conventional belief that Si(111) surfaces can not form a device-quality interface with SiO₂. We also found that surface step densities on vicinal Si(111), of the order of

10^6 cm⁻¹, make only minor additional contributions to these relatively low values of D_{it} .

2. Experimental

Experimental details have been described in previous publications[2,5]. Lightly-doped p-type Si wafers were first cleaned by the standard RCA method. For Si(100), the final sacrificial chemical oxide was removed by etching in 1.6 % HF, whereas Si(111) surfaces were treated in one of the three different solutions: 1.6 % HF, 1:6 BHF, and 40 % NH₄F. It is widely confirmed that the treatment in NH₄F produces an atomically-flat Si(111) surface while the HF treatment leaves a relatively rough surface[7]. After a short DI water rinse, the Si wafers were loaded into a multichamber remote plasma-enhanced CVD system where the two-step, 300°C process noted above was carried out. This process consisted of (i) an exposure to atomic-O generated by a remote O₂/He plasma, and (ii) remote plasma CVD to complete formation of ~10 to 20 nm SiO₂. The first step removed organic contamination at the Si surface, and at the same time formed a superficial oxide layer ~0.6 nm thick. After sputtering an Al electrode, the MOS structure was annealed in N₂ at 400°C for 30 minutes, and then was evaluated by the conventional high-frequency/quasi-static C-V method.

3. SiO₂/Si(100) Interfaces

The effectiveness of the two-step processing in achieving low D_{it} values on Si(100) is illustrated in Fig. 1, where D_{it} at midgap is plotted as a function of time of the atomic-O exposure. Without any exposure, i.e. $t = 0$, D_{it} shows considerable scatter between low 10^{10} and 10^{11} cm⁻².eV⁻¹ values. This is presumably due in part

to C residues on the Si surface and/or to excessive N incorporation at the interface[2]. After a 15 s exposure to atomic-O, D_{it} was reduced to the low $10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ range, essentially the same as what is typically observed for thermal oxide interfaces. The flat-band voltage was -0.60 V , which was in the range of what is estimated from the work-function difference between Al and the p-Si wafers. On-line AES of this pre-oxidized surface prior to SiO_2 deposition showed that there was no detectable C, and that the estimated oxide thickness was $\sim 0.6 \text{ nm}$. SIMS measurements showed that the C-atom concentration at the SiO_2/Si interface was $\sim 2 \times 10^{12} \text{ cm}^{-2}$, and the N-atom concentration was $\sim 1.5 \times 10^{14} \text{ cm}^{-2}$. No crystalline features were evident in the LEED measurement.

The D_{it} was almost unchanged upon longer exposures to atomic-O. This is in contrast to the case of atomic-H exposures, which are also shown in Fig. 1. D_{it} increases in proportion to time of the pre-deposition exposure to atomic-H, due to a roughening of the Si(100) surface.

MOSFET devices that incorporate the $\text{SiO}_2/\text{Si}(100)$ interfaces prepared by this process were fabricated[4], and display peak channel mobilities comparable to those of control devices incorporating a thermally-grown gate oxide.

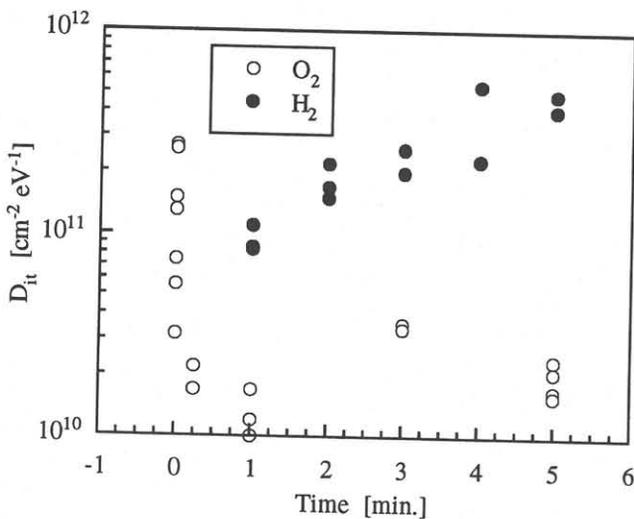


Fig. 1 D_{it} at midgap as a function of processing time for pre-deposition oxidation (open circles) and H_2 plasma cleaning (solid circles). The Si surface orientation was (100).

4. $\text{SiO}_2/\text{Si}(111)$ Interfaces

The two-step process consumes only a superficial layer of the Si wafer. It is qualitatively different from thermal oxidation, in which the Si substrate is consumed to create the oxide layer so that the SiO_2/Si interface is continuously regenerated during the process. Therefore, the two-step process provides for more control of the structure and bonding chemistry at the SiO_2/Si interface.

We have applied the two-step process to Si(111) surfaces where the structural integrity of the initial H-terminated surfaces can be readily controlled by varying the nature of HF/ NH_4F treatments used to remove wet chemical sacrificial oxides[7]. Prior to electrical evaluation of the MOS structures, we discuss the properties of Si(111) surfaces that were subjected to a treatment in three different HF/ NH_4F solutions. Figure 2 shows the imaginary part, ϵ_2 , of the pseudo-dielectric function of Si(111), $\langle \epsilon \rangle$, as determined by spectroscopic ellipsometry[6]. In SE, there is a basic rule that the greater the integrity of a semiconductor surface, the higher the ϵ_2 value for so-called E_2 transition peak (at 4.25 eV in Si). According to this rule, the NH_4F -treated surface has the highest integrity (i.e., it is the smoothest and the purest chemically) while the HF-treated one has the poorest. These observations are consistent with the IR, STM, AES, and LEED observations in the literature[5,7].

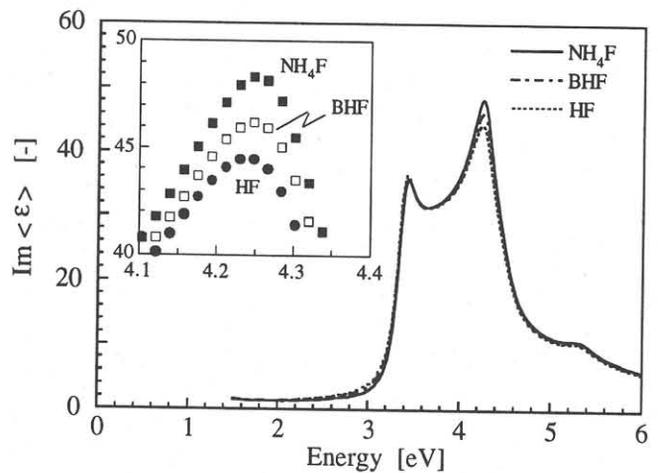


Fig. 2 Imaginary part of pseudo-dielectric function of Si(111) as determined by SE. The surface was treated in the three different solutions as indicated in the figure. The insert is a magnification of the values of ϵ_2 for the E_2 feature.

Figure 3 compares the D_{it} spectra of MOS capacitors on Si(111) that were subjected to the three different pre-deposition treatments. The lowest D_{it} was achieved with the NH_4F pre-deposition treatment, while the sample treated in HF showed the highest D_{it} . The overall trends in the figure are consistent with the changes in microstructure and chemical purity of the initial Si surface as reflected in the ϵ_2 spectra of Fig. 2. The D_{it} value at the midgap, $\sim 3 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, is significantly lower than those reported for thermally-grown $\text{SiO}_2/\text{Si}(111)$, typically high 10^{10} to $10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ [8], and is about as low as those obtained by F passivation of thermally grown $\text{SiO}_2/\text{Si}(111)$ [9]. The characteristic P_b -like feature at 0.3-0.4 eV could be further reduced by annealing in H_2 .

Since structural controllability of Si(111) surfaces

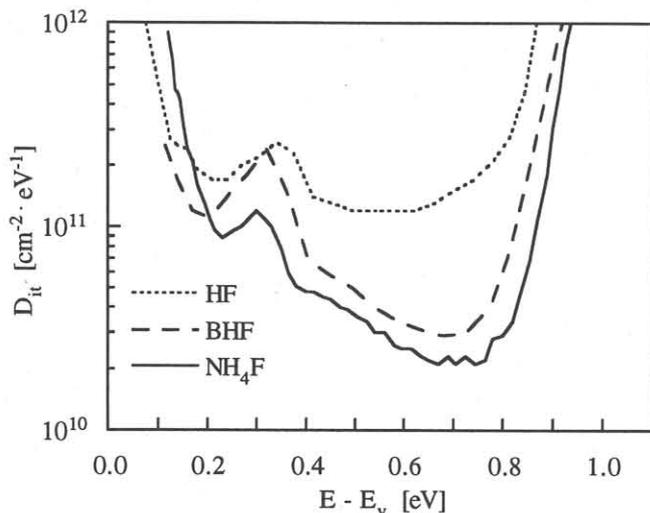


Fig. 3 D_{it} spectra of MOS capacitors fabricated on Si(111). The initial surfaces were subjected to the three different treatments as indicated in the figure.

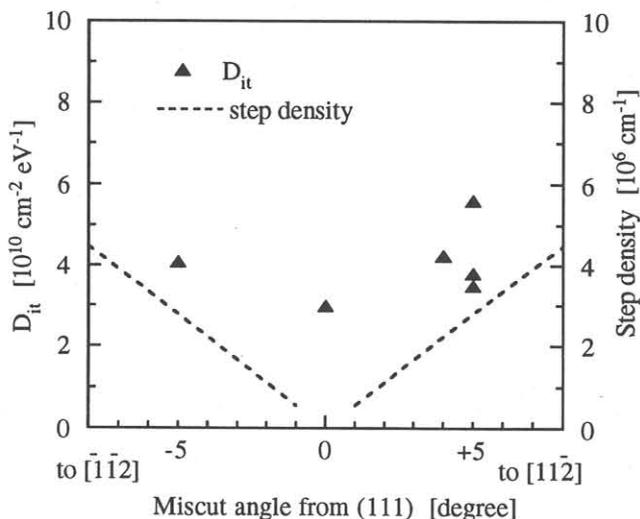


Fig. 4 Dependence of the midgap D_{it} on the miscut angle of Si(111). The initial Si surfaces were treated in NH_4F . The broken lines show the step density as calculated from the miscut angle.

are at most a minor contributor to D_{it} on Si(111) as long as their density is of the order of 10^6 cm^{-1} or less.

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References

- [1] J. Batey, E. Tierney, J. Stasiak, and T.N. Nguyen, *Appl. Surf. Sci.* **39**(1989)1
- [2] T. Yasuda, Y. Ma, S. Habermehl, and G. Lucovsky, *Appl. Phys. Lett.* **60**(1992)434; *J. Vac. Sci. Technol.* **B10**(1992)1844
- [3] Y. Kawai, N. Konishi, J. Watanabe, and T. Ohmi, *Appl. Phys. Lett.* **64**(1994)2223
- [4] V. Misra, S. Hattangady, T. Yasuda, X-L. Xu, B. Hornung, G. Lucovsky, and J.J. Wortman, *J. Vac. Sci. Technol.* **A12**(1994)1371
- [5] T. Yasuda, Y. Ma, Y.L. Chen, G. Lucovsky, and D. Maher, *J. Vac. Sci. Technol.* **A11**(1993)945; T. Yasuda, D.R. Lee, C.H. Bjorkman, Y. Ma, G. Lucovsky, U. Emmerichs, C. Meyer, K. Leo, and H. Kurz, *MRS Symp. Proc.* **315**(1993)
- [6] T. Yasuda and D.E. Aspnes, to be published in *Applied Optics*
- [7] G.S. Higashi, Y.J. Chabal, G.W. Trucks, and K. Raghavachari, *Appl. Phys. Lett.* **56**(1990)656; G.S. Higashi, R.S. Becker, Y.J. Chabal, and A.J. Becker, *Appl. Phys. Lett.* **58**(1991)1656
- [8] For example, E.H. Nicollian and J.R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982), p.792, and; C.H. Bjorkman, T. Yasuda, C.E. Shearon Jr., Y. Ma, G. Lucovsky, U. Emmerichs, C. Meyer, and H. Kurz, *J. Vac. Sci. Technol.* **B11**(1993)1521
- [9] X.W. Wang and T.P. Ma, *Appl. Phys. Lett.* **60**(1992)2634
- [10] T. Yasuda and D.E. Aspnes, *J. Vac. Sci. Technol.* **A12**(1994)1152

and $\text{SiO}_2/\text{Si}(111)$ interfaces was demonstrated in Figs. 2 and 3, we are now able to address some issues relating to the origin of D_{it} . One of these is the effect of surface steps. The step density on Si(111) can be controlled by varying the miscut angle of the crystal while keeping the terrace atomically smooth by the NH_4F treatment. Figure 4 shows the mid-gap D_{it} plotted as a function of the miscut angle. The local atomic structures at the steps are markedly different for the two miscut directions, $[\bar{1}\bar{1}2]$ and $[11\bar{2}]$ studied[10]. However, D_{it} is not strongly dependent on either the miscut direction, or the miscut angle. It is therefore concluded that surface steps