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Nitridation of SiO_2 in NO Ambient for Ultrathin Oxynitride Dielectric Formation

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In this paper, a novel technique for the formation of oxynitride gate dielectrics by *in-situ* rapid thermal NO-nitridation of SiO_2 is presented. This method allows for efficient incorporation of nitrogen (N) while minimizing the thermal budget. Growth kinetics related to NO-nitridation of SiO_2 is highly self limited due to the high N incorporation. The interfacial N is also responsible for excellent interface endurance, highly suppressed charge trapping and low-field leakage and superior breakdown characteristics.

INTRODUCTION

Recently, extensive research on various dielectrics has demonstrated the viability of oxynitrides in their application as gate and tunnel dielectric material. In particular, oxidation in N_2O ambient was found to be attractive due to the absence of hydrogen (H) in the processing ambient, which is a potential source of electron traps[1]. However, the levels of nitrogen (N) incorporated in the dielectric as a result of N_2O oxidation are low and inadequate to form an effective diffusion barrier[2]. In order to achieve higher [N] in the dielectrics by N_2O oxidation, a higher thermal budget is inevitable. Studies on the gas phase dissociation of N_2O had revealed that NO, which is one of the products of dissociation of N_2O is the species responsible for N incorporation in the dielectric[3,4]. However, the kinetics of N_2O dissociation show that the dissociation to NO is thermodynamically less favorable, since the bond energy of the N-NO bond (4.9 eV) is much higher than that of the N_2-O bond (1.67 eV)[5,6]. Hence, it appears that the direct reaction of NO with Si should result in higher [N] in the dielectric film compared to those from the reaction of N_2O with Si at the same temperature. In this paper, a new technique for the formation of high quality ultrathin oxynitride gate dielectrics, namely the nitridation of SiO_2 in pure NO ambient, is proposed and demonstrated for the first time. This method not only has the advantage of reduced thermal budget over N_2O oxidation, the resulting dielectrics also have reduced charge trapping and significant resistance to interface state generation under electrical stress.

While oxidation of bare silicon in N_2O ambient at 1050°C for 100 seconds produced 52Å oxide layer, oxidation in NO under the same conditions had grown only 25Å of oxide indicating that a higher [N] is incorporated in the latter case causing a slow growth rate. The higher [N] observed in the case of NO is probably due to the complete dissociation of NO into N and O and the reaction of these atomic species directly with silicon as opposed to the case of N_2O oxidation which, as explained above, is a less probable and indirect reaction. In order to demonstrate that larger [N] is incorporated in the silicon-oxynitride film through the oxidation of Si in NO, two thin oxide samples grown by oxidation of Si in NO and N_2O under identical conditions (1050°C for 18 seconds) were analyzed by x-ray photoelectron spectroscopy (t_{ox} <25Å). It is observed that the relative [N] in the NO-grown sample is one order of magnitude larger than that in the N_2O-grown oxide (Figs. 1a-b). This observation agrees well with the oxide growth data. The growth kinetics of NO-annealed SiO_2 is shown in Fig. 2. Initial thickness of furnace grown oxide layer were 49Å, 68Å and 89Å. The 1000°C, 80-second NO anneal increased the oxide thickness by only 3Å indicating the highly retarded growth kinetics associated with NO-grown oxynitrides.

EXPERIMENTAL

MOS capacitors with n^+-poly gate were fabricated with control and N_2O oxides (~52Å) which were grown in an rapid-thermal processing (RTP) chamber at 1050°C, and 1-atm in pure O_2 and pure N_2O ambient, respectively. NO-nitrided SiO_2 samples were prepared by growing an initial oxide layer (~ 45Å) by RTP in pure O_2 at 1050°C followed by *in-situ* nitridation in pure NO ambient at 1000°C and 1 atm.

RESULTS AND DISCUSSION

Initial device results, such as fixed charge density (N_f), flat-band voltage (V_{fb}) and initial interface state density (D_{it}) extracted from C-V data for NO devices

were somewhat higher than N_2O- and O_2-grown oxides, possibly due to higher N concentration (Table 1). J-E curves of devices with different gate dielectrics were overlapping with each other with slightly higher destructive oxide breakdown fields for NO-nitrided oxides (~14.5MV/cm) and N_2O-grown oxides (~14.7MV/cm) than that of pure SiO_2 (13.5MV/cm).

Fig. 3 compares the charge trapping properties of O_2-grown, N_2O-grown and NO-nitrided SiO_2. While O_2-grown oxides show highest amount of hole and electron trapping rates, N_2O oxides show suppressed trapping and NO devices show almost negligible charge trapping. N_2O-grown and NO-nitrided oxides have lower trapping rate, possibly due to the absence of weak Si-H bonds and the presence of Si-N bonds which replace strained Si-O bonds that can be easily broken during stress thus forming additional trap sites.

Fig. 4 shows the significant improvement in resistance to interface state generation (ΔD_{it}) observed in NO gate dielectric MOS capacitors compared to O_2-grown and N_2O-grown oxides. NO gate dielectrics have the highest immunity to interface state generation due to the highest concentration of N at the interface that replace strained Si-O bonds which are prone to bond breaking under electrical stress. Since under substrate injection, creation and propagation of defects to the SiO_2/Si interface dominates the mechanism for interface state generation, the strain gradient determines the amount of interface states generated. The N incorporation at the interface causes the SiO_xN_y/Si interface to be strainless, thus reducing the strain gradient across the film and retarding propagation of bulk defects to the cathode[7]. A higher amount of N incorporated at the dielectric/Si interface of NO-nitrided oxide reduces the strain gradient across the dielectric significantly, making these devices less prone to interface defect generation.

Fig. 5 shows Weibull plots for charge-to-breakdown (Q_{BD}) in capacitors with different gate dielectrics. NO nitrided oxides show largest Q_{BD}. The improvement in Q_{BD} can be attributed to the reduced charge trapping in NO-nitrided devices and the enhanced interface hardness at the SiO_2/Si interface. The N at the interface acts as barrier to migration of H atoms to the injecting interface thus protecting the dielectric from catastrophic breakdown by preventing softening of the interface[8,9]. The high values of Q_{BD} for NO-nitrided oxides are related to the higher amounts of N in the dielectric film which suppresses charge trapping and interface weakening. Superior Q_{BD} and immunity to ΔD_{it} of NO dielectrics should have significant potential for tunneling dielectrics application in EEPROM technology. The degradation in current versus voltage characteristics for MOS capacitors after subsequent injection of charge from the substrate is shown in Fig. 6. The stress-induced-leakage-current (SILC) is slightly lower in NO dielectrics compared with N_2O- and O_2-grown oxides. Low values of SILC is observed in the NO devices compared to N_2O- and O_2-grown oxides. SILC in thin oxides can be described as a field-assisted hopping of carriers from one trap to another and Yoon *et al.* have shown that there exists a strong correlation between ΔD_{it} and SILC[10]. Hence, it is believed that the interface quality is critical in determination of the supply of charge across the dielectric. Therefore, the suppressed degradation in SILC in NO devices can be attributed to the low ΔD_{it} in these devices. This property illustrates the potential of NO devices as reliable tunneling dielectrics.

CONCLUSIONS

Gate oxynitrides with excellent electrical properties formed by *in-situ* NO-nitridation of SiO_2 in an RTP system has been developed and characterized for the first time. This process is extremely attractive for ultrathin oxynitride formation due to its process simplicity, H-free nature, highly self-limiting growth and low thermal budget. Excellent interface endurance, charge trapping and breakdown properties make this technique attractive for ULSI technology. In addition, superior dielectric endurance and low field leakage make it desirable for tunnel oxide application. Highly effective barrier properties to boron diffusion allows for the use of this oxynitride gate dielectric for dual gate CMOS application.

ACKNOWLEDGEMENTS

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Samples	t_{ox} (Å)	N_f (cm^{-2})	V_{fb} (V)	D_{it} ($cm^{-2}eV^{-1}$)
NO-nitrided	54	18E10	-0.93	2.8E10
Pure N_2O-grown	52	14E10	-0.91	2.3E10
Pure O_2-grown	52	8E10	-0.85	1.0E10

Table 1 Initial electrical properties (N_f, V_{fb} and D_{it}) for different gate dielectrics.

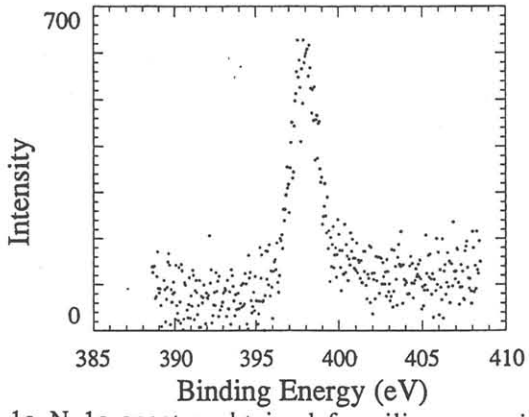

Fig. 1a N 1s spectra obtained for silicon-oxynitride grown by oxidation of Si in NO ambient at 1050°C for 18 seconds.

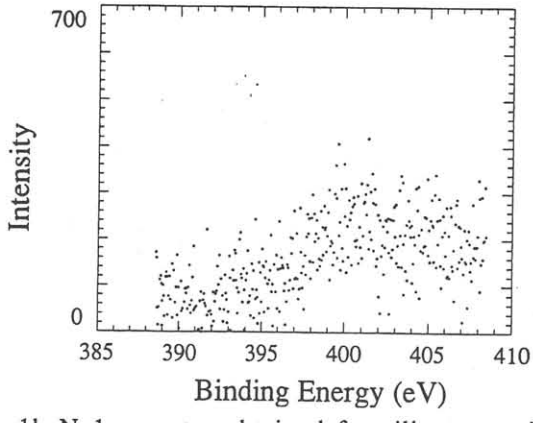

Fig. 1b N 1s spectra obtained for silicon-oxynitride grown by oxidation of Si in N_2O ambient at 1050°C for 18 seconds.

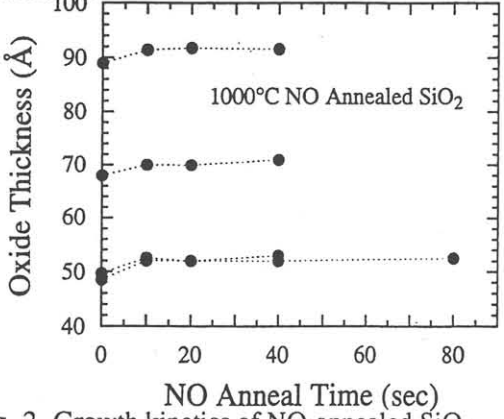

Fig. 2 Growth kinetics of NO-annealed SiO_2

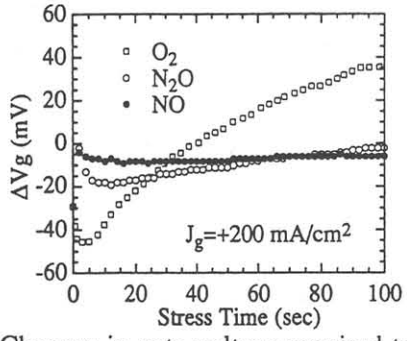

Fig. 3 Changes in gate voltage required to maintain a constant constant current density of 100mA/cm^2 in MOS (area: 5 x 10^{-5} cm^2) with different dielectrics

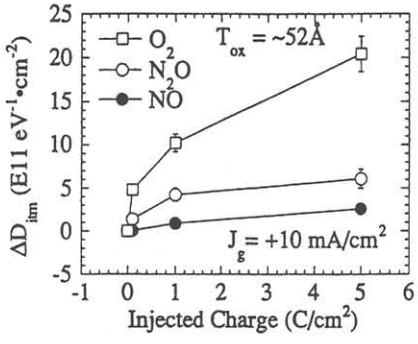

Fig. 4 Increase in midgap interface state density (ΔD_{it_m}) in MOS capacitors (area: 5 x 10^{-4} cm^2) with different gate dielectric materials, caused by F-N injection at a current level of 10mA/cm^2 under $+V_g$.

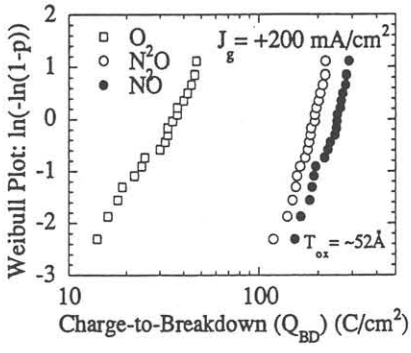

Fig. 5 Weibull plots of Q_{BD} in MOS capacitors (area: 5x10^{-5} cm^2) with different gate dielectrics, measured at a current density of 200mA/cm^2 under $+V_g$.

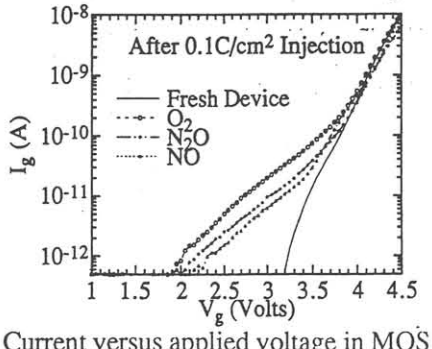

Fig. 6 Current versus applied voltage in MOS capacitors (area: 5 x 10^{-5} cm^2) with after injection of 0.1C/cm^2 of charge from the substrate.