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High Quality ONO Gate Dielectrics Fabricated by In-Situ RTCVD

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In this paper, we report for the first time, a novel ultrathin (<50Å) stacked $SiO_2/Si_3N_4/SiO_2$ (ONO) structure with the bottom and top oxides grown in N_2O ambient (N_2O-oxides) by *in-situ* rapid-thermal multiprocessing. Bottom N_2O-oxide was rapid-thermally grown and then Si_3N_4 film was deposited by *in-situ* rapid-thermal chemical vapor deposition (RTCVD) using SiH_4 and NH_3, followed by *in-situ* low pressure rapid-thermal N_2O-reoxidation of the nitride. A significant improvement in the interface endurance and resistance to boron penetration compared to conventional SiO_2 was observed. This is attributed to the exploitation of the respective advantages of the N_2O-oxide and nitride layers. The novel ONO gate dielectric is promising for the fabrication of p^+-polysilicon gated surface-channel p-MOSFETs.

1. INTRODUCTION

A major concern of p^+-polysilicon gate formed by BF_2 ion implantation is the boron penetration from the top polysilicon into the channel through the ultrathin gate oxide during thermal anneal [1]. This has been one of the important motivations to study other gate dielectrics such as oxynitrides [2] to replace conventional SiO_2. Oxynitrides have drawn considerable attention due to their superior electrical properties as compared to conventional SiO_2. Unlike NH_3-nitrided SiO_2, oxides grown in N_2O ambient (N_2O-oxides) [3] are very attractive due to the absence of hydrogen (H) in the processing ambient, which is a potential source of electron traps in the dielectric [4]. However, the low level of nitrogen (N) incorporated at the Si/SiO_2 interface as a result of N_2O oxidation is found to be insufficient to form an effective diffusion barrier to boron penetration [2]. In this paper, a novel technique for fabricating high quality ultrathin ONO gate dielectrics using N_2O-oxides as bottom and top oxide layers is proposed and demonstrated for the first time in order to improve the electrical properties, particularly the resistance to boron penetration. The novel ONO structure is found to have a significant improvement in the resistance to boron penetration mainly due to the excellent diffusion barrier property of nitride layer while maintaining reduced charge trapping and excellent interface endurance properties.

2. EXPERIMENTAL

MOS capacitors were fabricated on 5-10 Ω•cm P (100) or N (100) Si substrates. Substrates were chemically cleaned with RCA method. Prior to Si_3N_4 film deposition, bottom N_2O-oxides (20 Å) were grown in pure N_2O at 1050°C for 20 s. Si_3N_4 films (40 Å) were deposited in an RTCVD system with deposition pressure of 1.5 Torr at 800°C using SiH_4 and NH_3 (SiH_4/NH_3=1/20), followed by rapid-thermal reoxidation in N_2O ambient at 10 Torr at 1050°C for 30 s. Bottom N_2O-oxidation, silicon nitride deposition, and N_2O-reoxidation are sequentially performed by *in-situ* multiprocessing RTCVD [5]. Thickness of ONO gate dielectric is the oxide equivalent thickness (T_{eq}) calculated from the accumulation capacitance using the relative permittivity of silicon dioxide, 3.9. Furnace-grown thermal oxides in pure O_2 were used as control samples. The capacitors were completed by depositing ~4000 Å thick top poly-Si, $POCl_3$-doping, and patterning. The schematic cross section of the novel ONO stacked film capacitor is shown in Fig. 1. Electrical measurements were made on $POCl_3$-doped n^+-polysilicon gated MOS capacitors fabricated on p-type substrate. In order to study boron penetration, p^+-polysilicon gated MOS capacitors on n-type substrate were prepared by BF_2 implant ($5.5x10^{15}$ cm^{-2}, 20 KeV), followed by drive-in anneal in N_2 at several different temperatures for 30 min.

3. RESULTS AND DISCUSSION

Fig. 2 shows current-voltage (I-V) characteristics of the ONO gate dielectric in comparison with control oxide. The ONO dielectric with ultrathin (~ 40 Å) nitride layer shows almost comparable leakage current as the 45 Å control oxide. The bottom and top oxide layers have been reported to play critical roles in reducing leakage current in the nitride film due to the impeded hole injection from anode by the bottom or top oxides (> 30 Å) that is contiguous to the anode [6]. The relative

increase in conductivity is attributed to the very thin (< 20 Å) bottom as well as top oxides grown by low pressure (10 Torr) N_2O-reoxidation technique to avoid severe oxidation of ultrathin nitride film. As will be shown later, the advantage of using ultrathin nitride layer to fabricate the ONO structure is to suppress boron penetration without any degradation of other electrical and reliability properties.

The mid-gap interface state density (D_{it-m}) was extracted from the high and low frequency C-V data on capacitors with the ONO dielectric and control SiO_2. The novel ONO stacked gate dielectrics have been shown to have good interfacial characteristic (D_{it-m} = ~$3x10^{10}$ cm^{-2} eV^{-1}), comparable to the interface state density of control oxides. This suggests that the Si/SiO_2 interface in the ONO structure is preserved by the bottom N_2O-oxide. Interface state generations (ΔD_{it-m}) after 5 C/cm^2 charge injection under constant current stress (-10 mA/cm^2) are compared between the ONO and control oxide as shown in Fig. 3. The ONO stacked dielectrics show negligible distortion in low frequency C-V curve compared with control oxide, indicating excellent interface endurance of ONO layers. This is speculated to be due to the interfacial strain relaxation through the formation of SiO_xN_y at Si/SiO_2 interface during the bottom N_2O-oxide formation [3].

The gate voltage shifts (ΔV_g) required to maintain a constant current injection (200 mA/cm^2) under positive gate bias stressing were investigated as a function of stress time. Negative ΔV_g indicates internal electric field increase due to hole trapping near the cathode, whereas positive ΔV_g indicates electron trapping in the gate dielectrics. The highly suppressed electron trapping was observed in ONO gate dielectric whereas control oxide shows significant electron trapping as shown in Fig. 4. A significant amount of charge trapping in the bulk nitride as well as the oxide/nitride interface has been reported for thick nitride films. In this study, the nitride film is so thin that it can no longer trap charge effectively. Alternatively, detrapping of trapped charges in the nitride film is believed to be another contributing factor. This means that the electron trapping effect in the ultrathin nitride layer is not a great concern. Considering that charge trapping in the thick nitride has been a major problem to the success of gate dielectrics due to threshold voltage instability, the ultrathin ONO structure is suggested to be a good candidate for ULSI gate dielectrics.

Fig. 5 shows Weibull-plot distribution for time-to-breakdown (t_{bd}) data in n^+-polysilicon gated MOS capacitors with ONO dielectrics and control oxides. The novel ONO structures show longer t_{bd} values compared to control oxides, which can be attributed to the excellent interface endurance and suppressed electron trapping as shown in the Fig. 3 and 4, respectively. Fig. 6 shows a breakdown-voltage histogram for the ONO films (46 Å) obtained from ramp-voltage tests, which demonstrates no low field defects as well as relatively high average breakdown voltage. The RTCVD nitride layer in the ONO stacked dielectric is believed to play an important role in suppressing defect-related low field breakdowns [7].

To study the barrier properties of ONO gate dielectrics against boron penetration, flatband voltage (V_{fb}) shifts were investigated for BF_2-implanted p^+-polysilicon gated MOS capacitors with ONO gate dielectrics in comparison with control oxides. As shown in Fig. 7, flatband voltages (V_{fb}) of those MOS capacitors were plotted as a function of post-implant anneal temperatures, wherein V_{fb} becomes more positive with increasing anneal temperature. The positive V_{fb} shifts in these capacitors are attributed to a fully depleted layer of penetrated boron, located near the Si/SiO_2 interface [1]. Compared to control oxide, flatband voltage (V_{fb}) shift is very small for the entire range of temperature for the ONO sample, indicating the dominant role of nitride layer in suppressing boron penetration. The larger the amount of boron penetration, the larger are the positive V_{fb} shifts. Conclusively, ONO structures investigated here, show significantly suppressed boron penetration as compared to control oxides. It is believed that the ultrathin nitride layer in ONO structure plays a dominant role in suppressing boron penetration due to its excellent barrier property.

4. CONCLUSION

In conclusion, a novel ultrathin oxide/nitride/oxide (ONO) structures have been fabricated by combining the N_2O-oxide layer with the ultrathin nitride layer. The ONO structures have shown excellent interfacial characteristics and low defect density which are attributed to good interface formation by the N_2O-oxide with Si substrate and the high integrity of thin nitride layer, respectively. In addition, an excellent resistance to boron penetration is achieved mainly due to the good diffusion barrier property of nitride layer, which is desirable for the fabrication of p^+-polysilicon gated surface-channel p-MOSFETs.

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5. REFERENCES

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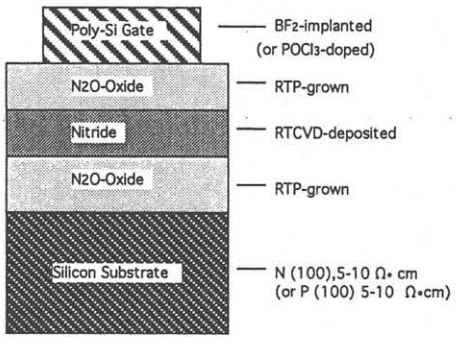


Fig. 1 Schematic cross-sectional view of the ONO stacked film capacitor.

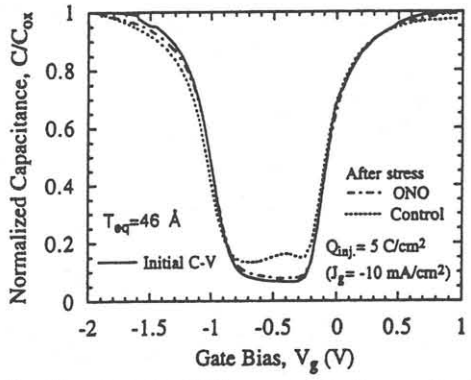


Fig. 3 Quasi-static C-V curves, before and after 5 C/cm^2 charge injection for n$^+$-polysilicon gate capacitors (area: 5x10^{-5} cm^2) on p-substrate with ONO dielectric (46 Å) and control oxide (45 Å).

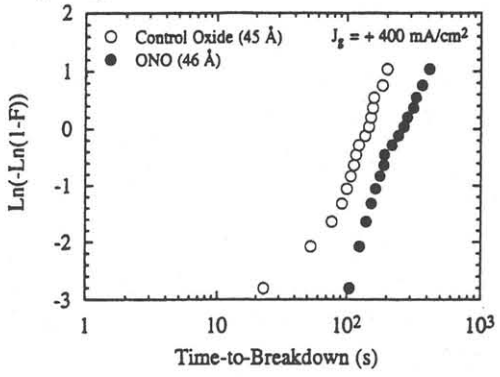
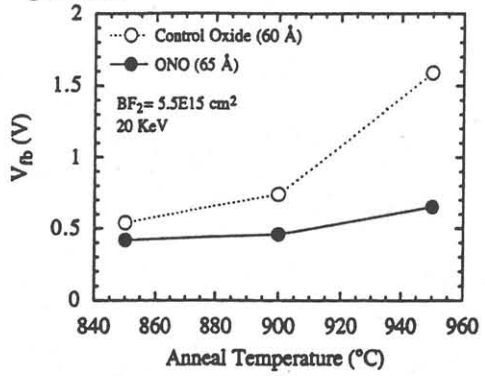


Fig. 5 Weibull-plots of time-to-breakdown (t_{bd}) in MOS capacitors (area: 5x10^{-5} cm^2) with ONO dielectric and control oxide, measured at a current density of 400 mA/cm^2 under positive gate bias.



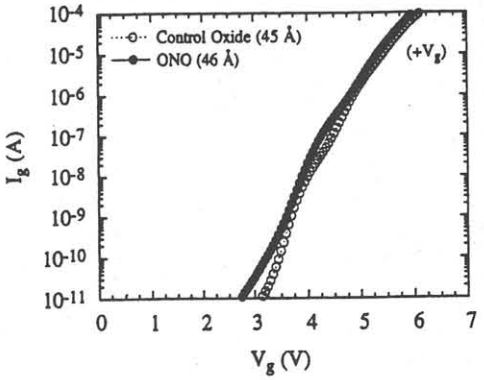


Fig. 2 Current vs. voltage (I-V) curves of n$^+$-polysilicon gate capacitors (area: 5x10^{-5} cm^2) on p-substrate with ONO dielectric and control oxide.

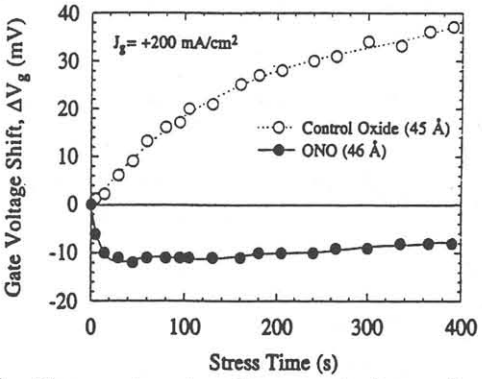


Fig. 4 Changes in gate voltage required to maintain a constant current density of +200 mA/cm^2 in n$^+$-polysilicon gate capacitors (area: 5x10^{-4} cm^2) on p-substrate with ONO dielectric and control oxide.

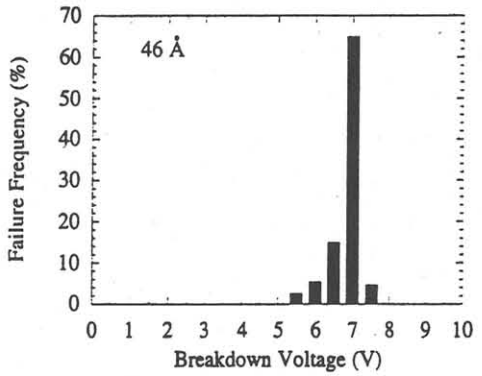


Fig. 6 Histogram of breakdown voltage for the 46 Å ONO stacked film capacitor.

Fig. 7 Flatband voltage (V_{fb}) in BF_2-implanted p$^+$-polysilicon gate MOS capacitors (area: 5x10^{-4} cm^2) on n-substrate with ONO dielectric and control oxide as a function of post-implant anneal temperatures.