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Low-Resistance $TiSi_2$ Formation by Controlling Si Surface Condition for Deep-Sub-Micron CMOS

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The silicon surface treatments were investigated to form low resistance $TiSi_2$ film, for deep-sub-micron CMOS devices. It was found that $TiSi_2$ films, formed after CDE treatment, APM,HPM cleaning and BHF dipping, showed the low sheet resistance, while $TiSi_2$ films, formed after only HPM cleaning, showed the higher sheet resistance. This sheet resistance dependence on Si-surface treatment is caused by the Ti-silicide formation suppression mainly due to the residual oxygen at the Ti/Si interface, and C49- to C54-$TiSi_2$ phase transition suppression mainly due to the oxygen in the $TiSi_2$ films. The low-resistance $TiSi_2$ film formation on narrow and highly-doped poly-Si lines was realized by the surface treatment to remove oxide from the amorphized Si surface.

Introduction

For deep-sub-micron dual-gate CMOS devices with self-aligned silicide (SALICIDE) process [1], the low-resistance silicide film ($\rho \leq 10\Omega/\square$) formation on the poly-Si gate and source/drain diffusion regions is required [2]. The C54 phase $TiSi_2$ film has the low resistivity of about $15\mu\Omega$·cm, compared with other silicide materials. However, it has been reported that it is difficult to form the thin and narrow C54-$TiSi_2$ film with low-resistance on the narrow poly-Si lines [3] [4] [5].

The silicide formation is generally affected by the metal/silicon interface state, and $TiSi_2$ growth has the incubation time of silicide formation for the Ti/Si systems with the silicon oxide at the Ti/Si interface [4]. Consequently, to be able to control the condition of Si surface is a critical issue, in order to form low-resistance $TiSi_2$ film on the narrower poly-Si. Thus, it is important to clarify the surface treatment effect before Ti deposition.

In this paper, the silicon surface treatments are investigated to form low-resistance $TiSi_2$ film. The $TiSi_2$ film formation on narrow and highly-doped poly-Si lines are also demonstrated, in connection with the silicon surface treatments.

Table 1: Experimental $TiSi_2$ film formation process flow

Process step	Conditions
substrate	P{100}, 13Ω·cm
SiO_2 deposition	10nm
dry etching	
O_2 plasma treatment	
surface treatments	sequences **A**,**B**,**C**,**D**,**E**
Ti deposition	35nm
1st RTA	665, 690℃, 30sec, in N_2 gas
selective TiN etching	20minutes
2nd RTA	810℃, 10sec, in N_2 gas

Table 2: Si-surface treatment sequences before Ti deposition

Sequence	Treatment
A	HPM($HCl/H_2O_2/H_2O$ mixture) cleaning
B	APM($NH_4OH/H_2O_2/H_2O$ mixture) and HPM cleaning
C	APM, HPM cleaning and BHF(buffered HF solution) dipping
D	CDE(chemical dry etching) treatment, APM and HPM cleaning
E	CDE treatment, APM, HPM cleaning and BHF dipping

Experiments

Table 1 lists the $TiSi_2$ film formation fabrication procedure to simulate the CMOS device fabrication. The 10nm-thick SiO_2, covering the p-type Si-substrate, was etched by the conventional dry etching. In order to remove CF_x layers deposited on the Si surface during dry etching, the samples were treated by O_2 plasma treatment [6]. One of the Si-surface treatment sequences before the Ti deposition, summarized in Table 2, was carried out. The $TiSi_2$ films were formed by the conventional 2-step rapid thermal annealing (RTA) process [1].

Five sequences **A-E**, combined four surface treatments, before the Ti deposition, were evaluated for the Si-surface condition control to form low-resistance $TiSi_2$ film. The HPM treatment makes thin oxide film on the Si-surface. The APM treatment and the BHF dipping are used to remove the surface oxide film. Chemical dry etching (CDE) treatment [6], featured by isotropic etching and low etching rate, is also used to remove the damaged Si layer, caused by SiO_2 dry-etching process.

No impurity doping into the Si was carried out for samples in Figs.1-5, in order to eliminate the $TiSi_2$ growth suppression by the dopant [7]. For evaluating the surface treatment effects on the $TiSi_2$ formation for the CMOS devices, $TiSi_2$ films on narrow poly-Si lines, doped with arsenic at $3\times10^{15}cm^{-2}$ dosage, were also prepared. To improve C49-to-C54 transformation for such highly-doped narrow lines, the pre-amorphization method was introduced before the surface treatment [8].

The sheet resistance was measured by the four probe method. The impurity depth profiles in Ti/Si and $TiSi_2$/Si systems and the crystal structures of $TiSi_2$ films were analyzed by secondary ion mass spectrometry (SIMS) and X-ray diffraction (XRD), respectively.

Results and Discussion

Figure 1 shows the sheet resistance dependence on the 1st RTA temperature for $TiSi_2$ film, formed on the unpatterned and undoped Si substrate, after the selective TiN etching. The sheet resistance of $TiSi_2$ film treated by sequence **A** was higher than those treated by other sequences. Figure 2 shows the sheet resistance dependence on the 1st RTA temperature for $TiSi_2$ film, formed on the unpatterned and undoped Si substrate, after the 2nd RTA. The $TiSi_2$ film sheet resistance treated by sequence **B** was higher than those treated by other sequences at the 1st RTA temperature of 665℃.

To investigate the $TiSi_2$ sheet resistance dependence on the Si surface treatment, impurity concentration in the $TiSi_2$/Si structure and $TiSi_2$ crystal structure were analyzed. Figure 3 shows that the 25nm-thick $TiSi_2$ film treated by sequence **A** is thinner than those treated by other sequences, after 2nd RTA. $TiSi_2$ films treated by sequences **B**, **C**, **D** and **E** have the same thickness of 35nm, approximately. Since the $TiSi_2$ thickness after 1st RTA is proportional to that after 2nd RTA, the higher sheet resistance of $TiSi_2$ film treated by sequence **A** is explained by the thinner film thickness, than those treated by other sequences, shown in Fig.1.

This SIMS analysis, furthermore, suggest that the highly-concentrated oxygen and nitrogen at the Ti/Si interface suppress the silicide formation to the C49-$TiSi_2$ film from the Ti/Si system, shown in Fig.3.

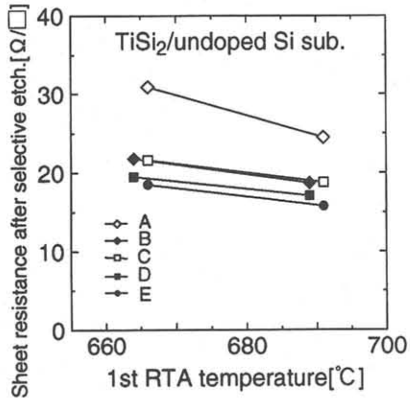


Fig.1: Sheet resistance dependence on the 1st RTA temperature after selective TiN etching.

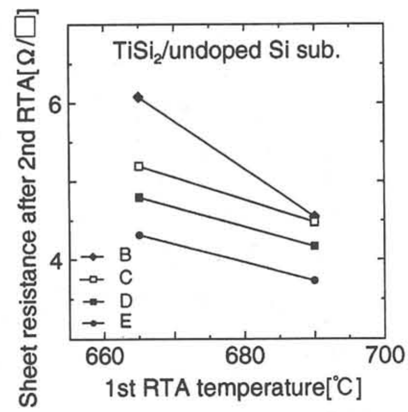
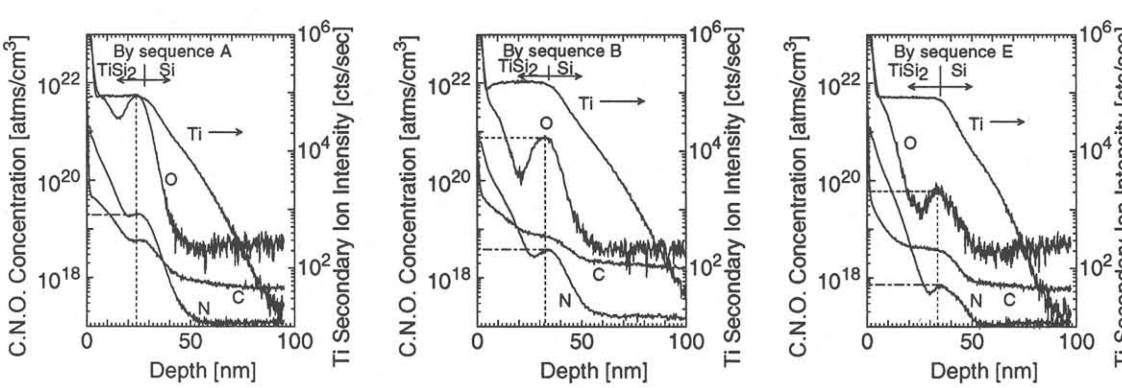


Fig.2: Sheet resistance dependence on the 1st RTA temperature after the 2nd RTA.



(a) By sequence **A** (b) By sequence **B** (c) By sequence **E**

Fig.3: SIMS depth profiles for titanium, oxygen, nitrogen and carbon in $TiSi_2$ films, after 2nd RTA at 810℃ with 1st RTA at 665℃.

Figure 4 shows the XRD intensity of C54 phase $TiSi_2$ films and oxygen concentration at the $TiSi_2/Si$ interface dependence on surface treatment sequences analyzed by XRD and SIMS, respectively. Figures 4 and 2 show that the higher XRD intensity of C54-$TiSi_2$ phase was observed for the $TiSi_2$ film with the lower sheet resistance value. Furthermore, the XRD intensity of C54-$TiSi_2$ phase is inversely proportional to the oxygen concentration at the $TiSi_2/Si$ interface. These results indicate that the phase transition from C49- to C54-$TiSi_2$ films can be restrained, due to highly concentrated oxygen and nitrogen at the $TiSi_2/Si$ interface. Therefore, it was found that the sequence **C**, **D** or **E**, removing the oxygen contamination at Si surface, are more effective to form the thin and low-resistance $TiSi_2$ films.

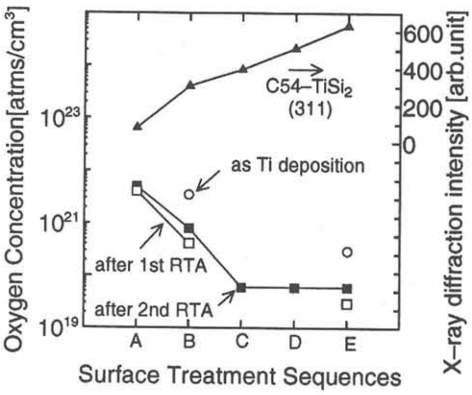


Fig.4: Surface treatment sequence dependence of oxygen concentration by SIMS depth profiles at the $TiSi_2/Si$ interfaces, and of X-ray diffraction intensity for C54-$TiSi_2$ films, after 2nd RTA at 810℃ with 1st RTA at 665℃.

For fine CMOS devices, it is important to form low-resistance $TiSi_2$ film on the narrow Si lines. Thus, $TiSi_2$ film on the narrow and undoped poly-Si lines are formed and characterized, in order to evaluate the Si-surface treatment effects without the dopant effect for the sheet resistance. In Fig.5, the $TiSi_2$ sheet resistances on undoped poly-Si, treated by sequence **C**, **D** or **E**, are 3-5Ω/□ lower than those by sequence **B**. This result clearly shows that the sequence **C**, **D** or **E** is effective for low resistance $TiSi_2$ films on narrow poly-Si lines.

Figure 6 shows line-width dependence of the $TiSi_2$ film sheet resistance on highly arsenic doped poly-Si lines, in order to demonstrate the appropriate Si-surface treatment for CMOS devices. The amorphization process [8], by using $3\times10^{14}cm^{-2}$ dosage arsenic ion-implantation was carried out to achieve the lower sheet resistance. The sheet resistances for $TiSi_2$ film treated by sequence **A** were remarkably high, while the sheet resistances for $TiSi_2$ film treated by sequence **E** were sufficiently low. It was found that the Si-surface treatment to remove oxide on amorphized Si surface is also effective for low-resistance $TiSi_2$ film formation on narrow and highly-doped poly-Si lines. $TiSi_2$ film with $\rho \leq 10\Omega/\square$ treated by sequence **E** can be realized for deep-sub-micron CMOS devices.

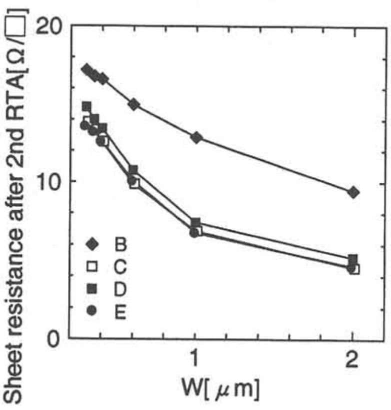


Fig.5: Sheet resistance dependence on the line width for $TiSi_2$ films on undoped poly-Si.

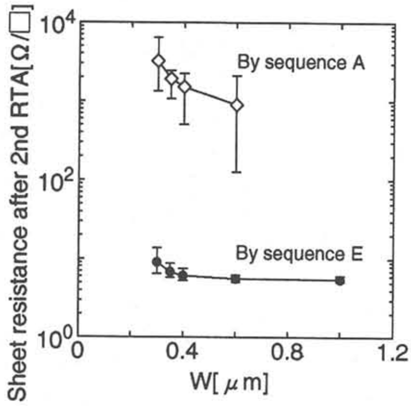


Fig.6: Sheet resistance dependence on the line width for $TiSi_2$ films, formed on the n^+ doped poly-Si, with amorphization by As ion-implantation.

Conclusion

The sheet resistance for thinner $TiSi_2$ films strongly depends on the Si-surface treatment. The sheet resistance surface treatment dependence was explained by the silicide formation suppression caused by the residual oxygen at the $TiSi_2/Si$ interface, and the phase-transition suppression caused by the residual oxygen in the $TiSi_2$ films. The low-resistance $TiSi_2$ film formation on narrow and highly-doped poly-Si lines was realized by the surface treatment to remove oxide from the amorphized Si surface.

References

[1] C.K.Lau et. al., IEDM Tech. Dig. 1982, 714.

[2] B.Davari, et. al., IEEE ED-39, No.4, 1992, 967.

[3] J.P.Gambino et. al., Abstract of ECS fall meeting, 1991, 312.

[4] Harrie J. W. van Houtum et. al., Mat. Res. Soc. Symp. Proc., vol.54, p.37, 1986.

[5] Jerome B.Lasky et. al., IEEE Trans. Electron Devices, vol.38 No. 2, p262.

[6] N.Aoto et. al., Ext. Abs. SSDM, p.101, 1993.

[7] Robert Beyers et. al., J. Appl. Phys. 61 (11), 1987.

[8] I.Sakai, et. al., Digest of VLSI Symp., 1992, 66.