

Novel Oxygen Free Titanium Silicidation (OFS) Processing for Low Resistance and Thermally Stable SALICIDE in Deep Submicron Dual Gate CMOS

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A low resistance and thermally stable TiSi_2 SALICIDE for deep submicron p^+ and n^+ dual gate CMOS has been developed. This was achieved through the use of a novel oxygen free silicidation (OFS) process using a reaction between a titanium nitride (Ti_xN_y) and an oxygen free Load-Lock LPCVD Si-gate. The OFS TiSi_2 film did not agglomerate after the treatment of the RTA at 1050 °C for 20sec. in a N_2 atmosphere and the additional furnace annealing at 900°C for 30min. in a N_2 atmosphere. For both n^+ and p^+ gates, low sheet resistances (about $2.8\Omega/\text{sq.}$) were achieved under the $0.2\mu\text{m}$ size.

1. INTRODUCTION

The development of a self-aligned silicide (SALICIDE) technique⁽¹⁾ is currently seen as the best candidate to reduce sheet resistances of transistor source / drain, and gate electrodes in deep submicron ULSI. In particular, the titanium SALICIDE process is one of the most promising techniques for deep submicron p^+ and n^+ dual gate CMOS. However, it is quite difficult to form the TiSi_2 layer with low resistance and high temperature stability on a deep submicron gate. When aiming for shrinkage of pattern dimension, two problems present themselves; the difficulty in achieving phase transition from C49 to C54 at around the low temperature of 800°C, and the acceleration of agglomeration^(2,3). The thermal stability is affected by oxygen concentration in the silicon and titanium layers, and their interface region before the silicidation reaction^(4,5). Furthermore, the presence of oxygen prevents the silicidation reaction.

As a means of ultimately overcoming these problems, we developed a novel oxygen free silicidation (OFS) process using a reaction between a titanium nitride (Ti_xN_y) and an oxygen free Load-Lock LPCVD Si-gate. In this process, an impurity ion implantation was performed after the silicidation reaction, to eliminate the problem of knocked on oxygen in the silicon layer introduced by the ion implantation through the oxide layer before silicidation⁽⁵⁾. By using this novel OFS process, the TiSi_2 film did not agglomerate after the treatment of the RTA at 1050 °C for 20sec. in a N_2 atmosphere and the additional furnace annealing at 900°C for 30min. in a N_2 atmosphere. Taking advantage of this property, low sheet resistance (about $2.8\Omega/\text{sq.}$) was achieved under the $0.2\mu\text{m}$ size for both n^+ and p^+ gates by the treatment of the RTA at 1000°C. In the n-channel LDD structure (1000Å sidewall thickness) employing the OFS process, series resistance

was about 50% lower than the conventional case (without SALICIDE). The maximum transconductance values (G_m) in the linear and saturation regions were both improved by about 45%.

2. EXPERIMENTAL

A comparison of the fabrication sequence for the novel OFS process and the conventional process is shown in Fig. 1. The SALICIDE process employed a 2-step rapid thermal annealing (RTA) with halogen lamp heating in a N_2 atmosphere⁽⁶⁾.

In the conventional process, the gate poly-Si was deposited using a conventional LPCVD system. After the gate electrode and side wall spacer formation, a cap oxide layer was deposited and a impurity ion was implanted through the cap oxide layer. Activation annealing was then carried out at 900°C for 10min. in a N_2 atmosphere. The Ti film with 50nm thickness was deposited after removing the cap oxide by HF based solution. The first step RTA was performed at 625°C for 20sec. in a N_2 atmosphere. After the first low temperature RTA, the titanium nitride and unreacted Ti were etched off by a H_2SO_4 based solution, followed by the second step high temperature RTA at 850°C for 20sec. in a N_2 atmosphere for the final silicidation.

In the OFS process, the gate poly-Si was deposited using a Load-Lock LPCVD system. The oxygen concentration in a poly-Si film deposited using a Load-Lock LPCVD system was under the detection limit, as shown in Fig. 2. After the gate electrode and side wall spacer formation, the Ti_xN_y film was deposited by reactive sputtering method (1% N_2 + 99% Ar) using an ultra high vacuum DC magnetron sputtering multi-chamber system, followed by first step low temperature RTA at 625°C for 20sec. in a N_2 atmosphere without atmospheric exposure.

The base pressure of this system was under the 1×10^{-8} Torr. The impurity ion implantation was performed through the titanium nitride layer. After selective etching of the titanium nitride and unreacted Ti_xN_y layer, the second step RTA was carried out at 1000°C for 20sec. in a N_2 atmosphere.

3. RESULTS AND DISCUSSION

Figure 3 shows sheet resistances of the $TiSi_2/n^+$ -poly-Si films formed by the OFS and conventional silicidation processes as a function of the second step RTA temperature. The first step RTA condition was fixed at 625°C for 20sec. in a N_2 atmosphere. In the conventional sample, the sheet resistance increased at over 950°C . This indicates that the $TiSi_2$ film formed by the conventional process was agglomerated at over 950°C . On the other hand, the sheet resistance remained stable at about $2.8\Omega/\text{square}$ at over 1000°C in the OFS sample. Figure 4 shows the SEM images of the $TiSi_2$ layers around the gate electrode formed by the OFS and conventional silicidation processes after the second step RTA at 1050°C for 20sec. in a N_2 atmosphere. It can be clearly seen that the OFS SALICIDE did not agglomerate at 1050°C . These results indicate that the OFS process achieved desirable thermally stable characteristic, which is necessary to transform the crystal structure of $TiSi_2$ film from C49 to C54 on the deep submicron gate.

Figure 5 shows the X-ray diffraction patterns for $TiSi_2$ layer formed by the conventional and OFS processes. The second RTA was performed at 1000°C in both processes. The crystal structure of $TiSi_2$ C54 was not changed even for the agglomerated sample (conventional process). The difference between the agglomerated sample (conventional) and the non agglomerated sample (OFS) was only a crystalline orientation. Based on these results, it seems that the agglomeration is caused not by a chemical reaction with a change in crystal structure but by a phenomena to minimize surface free energy of $TiSi_2$ grain. A model of the agglomeration mechanism is shown in Fig. 6. Using the OFS process, agglomeration was suppressed at high temperature annealing above 1000°C . In this case, we propose that in the $TiSi_2$ structure formed by the OFS process, a reaction between Ti_xN_y and Si caused the formation of TiN in the $TiSi_2$ grain boundary. On the other hand, we believe oxide exists in the $TiSi_2$ grain boundary in the conventional case. The agglomeration results are explained in terms of the introduction of the surface free energy between the $TiSi_2$ and SiO_2 which was much higher than that between the $TiSi_2$ and TiN.

Figure 7 shows the SEM images for the surface morphology of $TiSi_2$ films formed by the conventional and OFS processes after furnace annealing at 900°C for 30min. in a N_2 atmosphere. The furnace annealing was performed after the deposition of an insulator layer to prevent the oxidation of the $TiSi_2$ surface. To observe the surface morphology of $TiSi_2$ films, the insulator layer was removed by reactive ion etching (RIE). It was confirmed that the surface morphology was smooth and no agglomeration occurred in the OFS sample. On the other hand, the agglomeration occurred in the conventional

sample. By using the novel OFS process, it was possible to realize the additional furnace annealing at around 900°C after the silicidation process. This additional furnace annealing is important to reflow the BPSG insulator layer.

Figure 8 shows the sheet resistances of the n^+ and p^+ -gates formed by the OFS process as compared with the conventional silicidation on n^+ gate as a function of the gate length. The low sheet resistances were maintained at under $0.2\mu\text{m}$ gate length for both n^+ and p^+ .

Figure 9 shows the I_D-V_D characteristics of the OFS-SALICIDE LDD-NMOSFET and conventional LDD-NMOSFET (without SALICIDE) with a physical gate length of $0.26\mu\text{m}$. Gate oxide thickness was 5.0nm , and gate sidewall thickness was 100nm . It was confirmed that high drivability was achieved. In the OFS transistor, the maximum transconductance ($V_{DD}=2.0\text{V}$) values in the linear and saturation regions were about $73.7\mu\text{S}/\mu\text{m}$ and $302.1\mu\text{S}/\mu\text{m}$, respectively. Furthermore, the series resistance in OFS transistor was about $576.5\Omega\text{-}\mu\text{m}$. These results indicate a 45% improvement for the G_m in both the linear and saturation regions, and a 50% reduction in series resistance as compared with the conventional case (without SALICIDE), as shown in Table 1.

4. CONCLUSIONS

A novel oxygen free silicidation (OFS) process for deep submicron dual gate surface channel CMOS has been demonstrated. By using this process, the $TiSi_2$ film did not agglomerate after the treatment of the RTA at 1050°C for 20sec. in a N_2 atmosphere and the additional furnace annealing at 900°C for 30min. in a N_2 atmosphere. Taking advantage of this property, low sheet resistance (about $2.8\Omega/\text{sq.}$) was achieved under the $0.2\mu\text{m}$ size for both n^+ and p^+ gates by the treatment of the RTA at 1000°C . In the n-channel LDD structure (1000\AA sidewall thickness) employing the OFS process, series resistance was about 50% lower than the conventional case (without SALICIDE). The maximum transconductance (G_m) values in the linear and saturation regions were both improved by about 45%.

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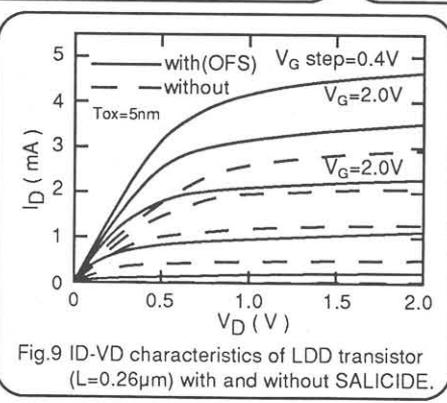
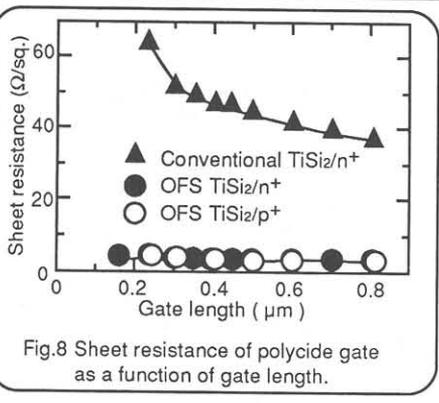
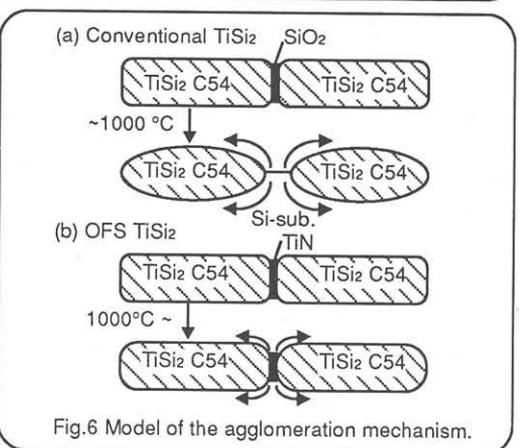
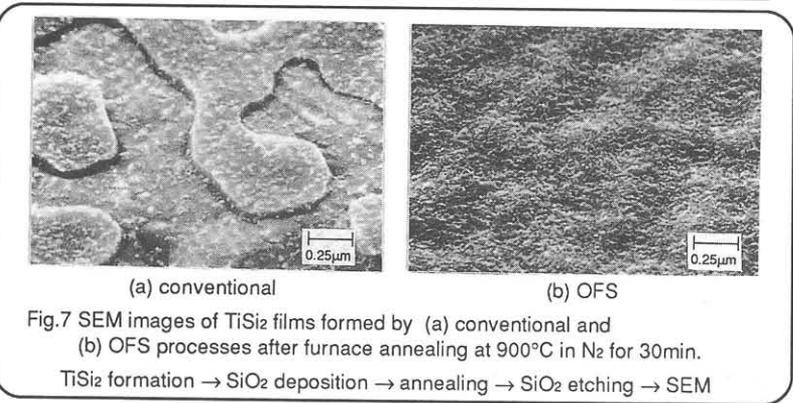
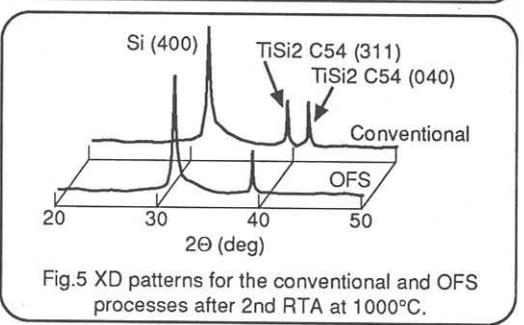
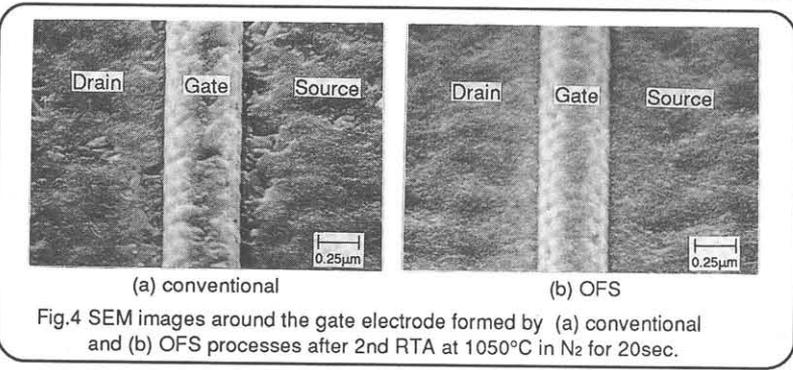
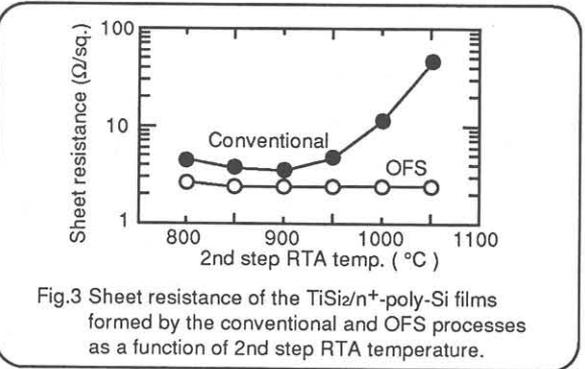
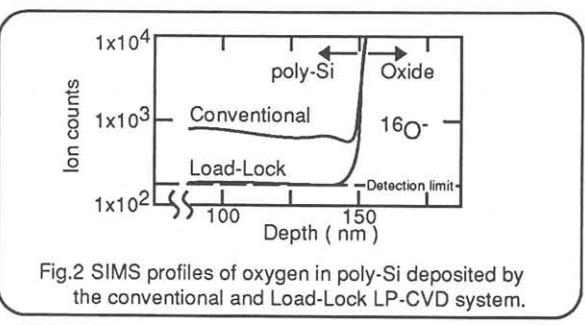
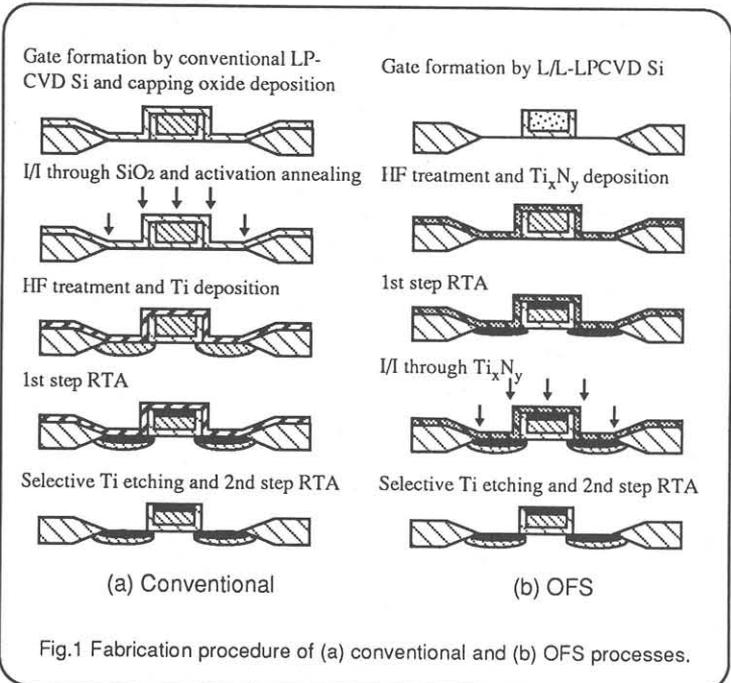


Table.1 Transconductance and series resistance of LDD transistor with and without SALICIDE.

L=0.26μm Tox=5nm	without	with (OFS)
Gm (V _{DD} =2.0V) (linear)	51.4 μS/μm	73.7 μS/μm
Gm (V _{DD} =2.0V) (saturation)	207.5 μS/μm	302.1 μS/μm
Series resistance	1252.5 Ω-μm	576.5 Ω-μm