Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 871-873

Invited

Silicon: Germanium Heterojunction Bipolar Transistors; From Experiment to Technology

B. S. Meyerson, D. L. Harame, M. M. Gilbert, K. T. Schonenberg
T. Tice+, and B. Scharf+

IBM Research Division, IBM T. J. Watson Res. Cntr.
P.O. Box 218, Yorktown Hgts., NY. 10598, USA
+Analog Devices Inc.
Greensborough, NC. 27409 USA

Recent advances in thin film growth techniques, combined with refinements in heterojunction bipolar transistor designs, have led to the first integrated circuits in the silicon:germanium materials system. Utilizing a commercial(Leybold-AG) UHVCVD tool for SiGe epitaxy on an otherwise standard 8" CMOS line, waferscale integration is achieved, the first IC components being 1-Ghz, 12-bit, digital to analog converters.

1. INTRODUCTION

Heterojunction bipolar transistors(HBT) have been known for decades, and have been executed in several of the III-V material systems, most commonly GaAs/GaAlAs. These devices have found niche markets in military applications, as well as more common applications at the high end of the frequency spectrum where silicon homojunction bipolar devices did not achieve the required levels of performance. Advances in silicon:germanium(SiGe) based HBT's in the late 80's demonstrated[1] extraordinary gains in device performance, but SiGe IC development lagged.

The fundamental difficulty in developing SiGe based IC's has been the inherent strain induced in the growth of SiGe alloys commensurate to a silicon substrate. The 4% lattice mismatch between Si and Ge leads to stringent limits upon the thickness to which a layer of given Ge fraction may be deposited before relaxation occurs by dislocation formation. These limits are shown in figure 1, where both the theoretical[2](Matthews and Blakeslee) and empirical[3] limits(defects found after a 900C 30 minute anneal) of SiGe film thickness on silicon are shown. Effective strain is the percent lattice mismatch between the film and substrate. To insure the viability of devices employing a SiGe base layer, several simple strategies were devised.

a) Design SiGe/Si heterojunction devices exacting the maximum performance gain for a given level of Ge content/strain.
b) Utilize low temperature epitaxy for SiGe base deposition, emphasizing the control required to achieve a stable/manufacturable process.
c) Restrict device implementations to those that are fully compatible with standard CMOS waferscale processing and integration.

2. DEVICE DESIGN CONSIDERATIONS

Following the strategies stated above, the double heterojunction graded bandgap HBT was selected as the standard device in this program. The band structure of such a device is shown in figure 2, and was chosen to make the most efficient use of a given dose of Ge contained within the base of the device. The primary gain in device performance utilizing this structure is obtained by a reduction in the base transit time(T_B), made possible by a built-in potential. The field across the base of the device is of order 30-50kV/cm., resulting in approximately a factor of two reduction in T_B for a given base geometry. Taken to the extreme of a 0-25% Ge ramp across a 300Å basewidth, values[4] of unity gain cutoff frequency(f_T) are in the range 110-117Ghz.

Although long employed in GaAs/GaAlAs HBT's, it has recently been reported[5] that one may employ a uniform, or box-like Ge profile in a SiGe base HBT, and also achieve high performance SiGe HBT's. However, in the absence of a built-in potential, such designs utilize several times the Ge content[5, 6] of graded base devices to achieve similar levels of performance. The added strain has been shown[3] to result in a dense network of dislocations, of density $>10^6 cm^{-2}$, when such devices are exposed to temperatures significantly in excess of their growth temperature, typically 500-700C. This level of strain renders such devices fundamentally incompatible with conventional silicon processing and integration techniques. This restriction has precluded the integration of such devices at modern levels of complexity.

A second issue related to device design is the issue of dopant profile. A common method employed for the reduction of band to band tunneling in heavily doped bipolar devices, since the advent of epitaxial base devices, has been the use of intrinsic spacer regions at the base-collector[7, 8] and base-emitter junctions[9]. Lightly doped junctions result in lower leakage, higher breakdown voltage, as well as reduced parasitic capacitances. It was been shown[8] that the addition of a significant intrinsic spacer to the base collector junction increases BV_{ceo} while leading to minimal degradation of the unity gain cutoff frequency due to the increase in vertical device dimensions. A similar intrinsic region has been employed to space the emitter away from the base of the device, this having been demonstrated for SiGe base HBT's of both graded[9], and more recently[5] uniform Ge profiles. In that clean device characteristics over ten decades of current were obtained with the utilization of only the base collector spacer, this was the dopant strategy employed, with a conventional polysilicon emitter formed directly above the base of the device.

3. Fabrication and Integration

For the purpose of integration, the device structures employed in the present work all employ substrates with patterned isolation and other requisite features for IC fabrication. The SiGe base profiles employed in this work were deposited employing a commercial Leybold-AG UHVCVD[10] apparatus(figure 3) at temperatures in the range 500C<T<550C. The structure of the device, as well as the route taken to full integration, is seen in figure 4. Most notable is the side by side compatibility with standard CMOS, as well as other standard passive elements such as resistors(shown here), capacitors, inductors, etc.

In the course of this effort, we have explored the adaptation of this heretofore "digital" technology to a variety of analog applications. In a recent report[11] we detailed the device performance of a variety of Ge profiles optimized for analog application, and for brevity here I refer the reader to that text. However, an important finding of this work is reported at this later date.

4. Devices

In exercising a variety of graded Ge profiles, an important aspect in the behavior of such HBT's is demonstrated. Figure 5 shows the temperature dependence of β for an HBT with a trapezoidal Ge profile over the temperature range 25-125C. The total variation across this range is found to be <10%. Examining the behavior of all profiles explored, it was found that β for a device employing a triangular(as in figure 2) Ge profile was temperature invariant(±5%). The virtual absence of temperature dependence in this SiGe HBT stems from the matching of base bandgap reduction via Ge inclusion with emitter bandgap reduction due to heavy doping effects. The net result is a temperature invariant device over a wide range.

5. Circuits

The ultimate test of the viability of a technology is reduction to practice in integrated circuits. A high speed 12-bit SiGe HBT based DAC was reported[11] at IEDM'93 using this technology, and its dynamic response to a full scale code shift, 0 to 4096, is shown in figure 6. The DAC settles in less than 900ps., as required in the 1Ghz. design, yet consumes less than 1 watt at speed. More detailed data on phase noise and other characteristics will be presented at a later time.

6.Summary

We have detailed the reduction to practice of SiGe HBT's as an IC technology. Employed a UHVCVD grown epitaxial base, in an 8" waferscale integration technology, we have demonstrated medium scale IC performance well beyond the state of the art for silicon technology, and well beyond the power-delay product performance available in III-V based devices.

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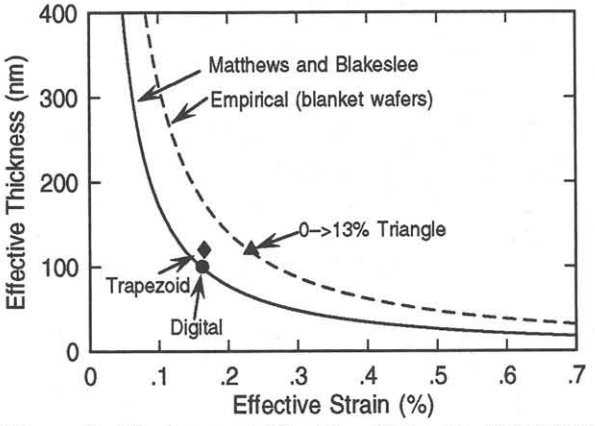

Figure 1. Maximum stable film thickness, theoretical and empirical, for films of a given percentage lattice mismatch(1%=$Si_{0.75}Ge_{0.25}$). Points show the location of several Ge profiles explored&@citstr(). in this application.

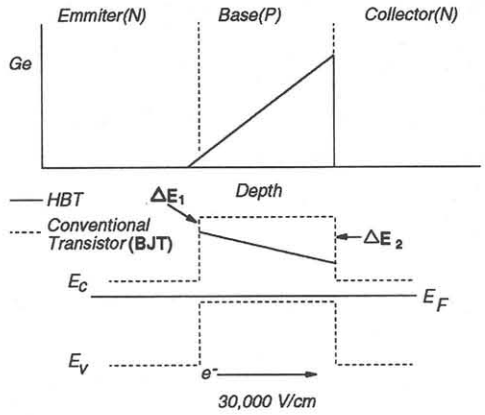

Figure 2. Band structure in a graded bandgap SiGe HBT with Ge profile as shown above.

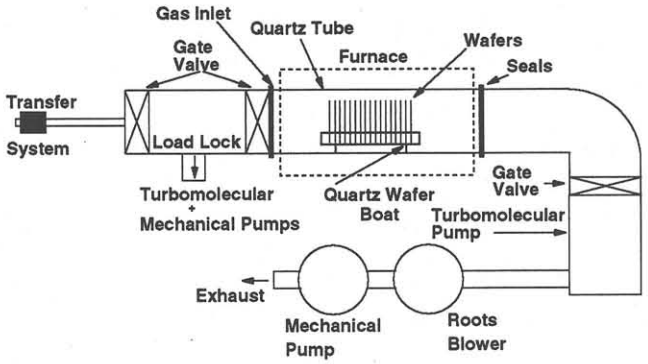

Figure 3. A schematic of the UHVCVD system employed in this work.

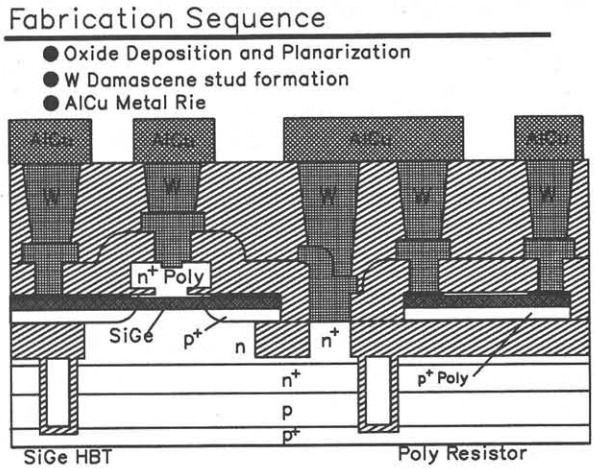

Figure 4. SiGe HBT integration technology shown in cross-section. Fabrication sequence is for the first of 3 to 4 levels of metallization

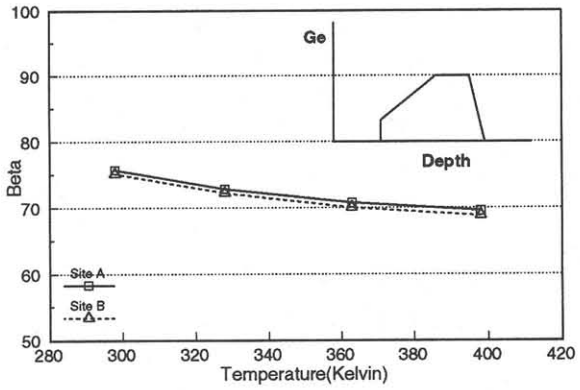

Figure 5. Transistor gain versus temperature for a trapezoidal Ge profile(see inset) SiGe HBT.

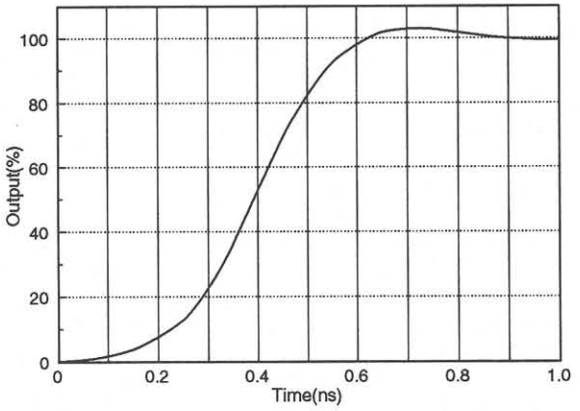

Figure 6. Full scale(0-4096) response for 12-bit SiGe HBT DAC.