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Modelling and Fabrication of a P-Channel SiGe-MOSFET with Very High Mobility and Transconductance

T. Vogelsang, F. Hofmann, H. Schäfer, L. Risch and K. Hofmann*

Siemens AG, Central Research and Development BT ACM

Otto-Hahn-Ring 6, 81739 Munich Germany

We have fabricated p-channel MOS transistors with SiGe-channels grown by selective epitaxy and gate lengths down to 0.4μm in a standard CMOS logic production line. Device performance is significantly enhanced by the SiGe-channel. For comparison with experimental data a mobility model for SiGe was developed. We take into account the reduction of hole effective mass and alloy scattering. We have shown that the influence of increased mobility and of quantum confinement in the SiGe-channel is of similar size.

1. Introduction

A key problem for CMOS logic is the poor driving capability of the p-channel transistor compared to the n-channel transistor. The confinement of holes in a buried SiGe-quantum well with higher mobility is a possible way to solve this problem.[1] We have fabricated p-channel MOS transistors with gate lengths down to 0.4μm utilizing a $Si_{1-x}Ge_x$ layer to enhance device performance. We have simulated the devices to provide a better understanding and make further improvements possible. To that purpose we have developed an extension of the standard low field mobility model of Arora[2] to allow for the change of hole mobility in SiGe. The new model takes into account the reduction of hole effective mass and alloy scattering as an additional scattering mechanism.

2. Experimental

The devices were made in a 0.6μm CMOS logic production line with selective SiGe-CVD epitaxy as an additional process step, a low temperature gate oxide (750°C) and RTP annealing (950°, 10s) of source and drain implantation to keep the thermal budget small. Some of the devices also include a boron doped layer for threshold voltage control. Fig. 1 shows a TEM photograph of the device structure with dimensions of 15nm $Si_{0.8}Ge_{0.2}$, 2.5nm Si cap and a gate oxide thickness of 5 nm. To identify the influences of different parameters, we compare the data of transistors with a $Si_{0.8}Ge_{0.2}$ layer both with and without boron doping to transistors without this layer which were otherwise fabricated in the same technology. Boron doping of the channel was achieved by the epitaxial growth of a boron doped delta layer below the SiGe-layer.

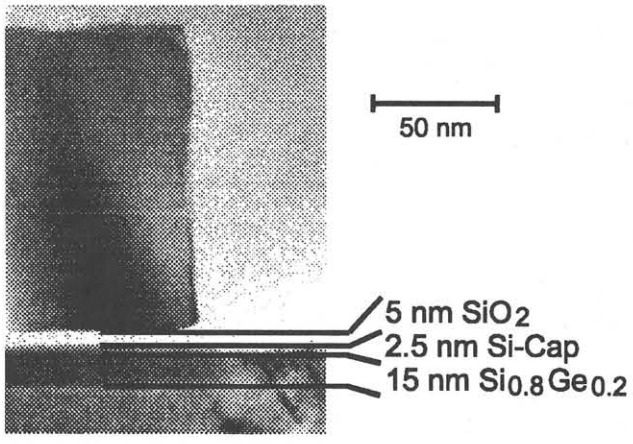

Fig. 1: TEM photograph of SiGe-Quantum-Well-MOSFET structure.

Both SUPREM III simulation and SIMS measurements show a nearly uniform boron distribution after processing of the device due to the high diffusion of boron even at comparatively low temperatures. SUPREM III simulation shows also that a layer of phosphorous was formed below the gate oxide during implantation and annealing of the n-poly gate. This is

* University Hannover, Institute for Semiconductor Technology, Appelstr. 11a, 30167 Hannover

confirmed by good agreement of simulation and experiment for long channel threshold voltages of devices without boron and SiGe layers. Fig. 2 shows the distribution of impurities and germanium at a cross section through the channel. The transconductance of 180mS/mm at room temperature for the 0.4µm gate length device is to our knowledge the highest value reported for this type of device. Maximum effective mobility for 2µm gate length is 110cm^2/Vs resp. 200cm^2/Vs for a temperature of 298K resp. 98K compared to 65cm^2/Vs resp. 127cm^2/Vs for a silicon channel.

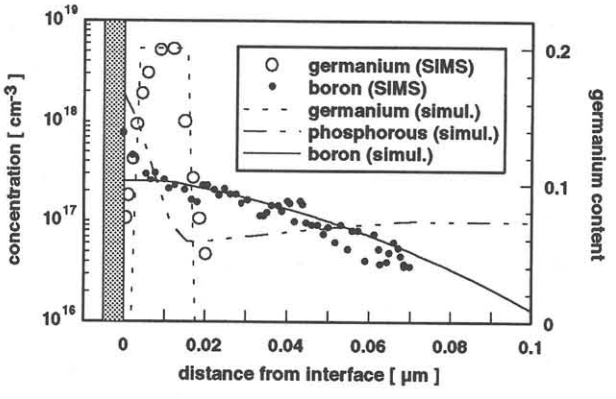

Fig. 2: Doping concentration and germanium profile - dots: SIMS data, lines: simulation profiles

3. Theory

For device simulation it is necessary to take into account the changed mobility in a SiGe-layer. We have developed a model which can be used as an extension to the usual models in commercially available drift diffusion simulators. For use in drift diffusion simulators the model has to be simple and to depend only on the most important changes due to the material SiGe. These are the reduction of hole effective mass and alloy-scattering as a new scattering mechanism. The change of hole effective mass in strained SiGe was computed by kp-theory. To first order its influence can be taken into account by multiplication of the Arora mobility with the ratio of the effective conduction masses of Si and SiGe. We used Rode's Legendre expansion technique[3] to calculate the strength of alloy scattering. The modified Arora mobility and the mobility due to alloy scattering were combined using Mathiesen's rule. The results were fitted with the formula below and implemented in the drift diffusion simulator ATLASII/BLAZE[4].

$$\mu_{LI}(x,T,N_I)=\mu_{Arora}(T,N_I)\cdot(1+4.31x-2.28x^2)$$

$$\mu_{LIA}(x,T,N_I)=\left[\frac{1}{\mu_{LI}(x,T,N_I)}+\frac{1}{\mu_A(x)}\right]^{-1}$$

$$[\mu_A(x)]^{-1}=\begin{cases} x(1-x)\exp(-7.68x)\Big/124.1\dfrac{cm^2}{Vs} & ,x\le 0.2 \\ \exp(-2.58x)\Big/2150\dfrac{cm^2}{Vs} & ,0.2<x<0.6 \end{cases}$$

Fig. 3 shows a comparison of our model with the calculations of Manku et. al.[5] The differences at doping levels between 10^{17} cm^{-3} and 10^{18} cm^{-3} result from the Arora model as basis of our SiGe model. We keep the doping dependence of that model because of the good results for silicon devices.

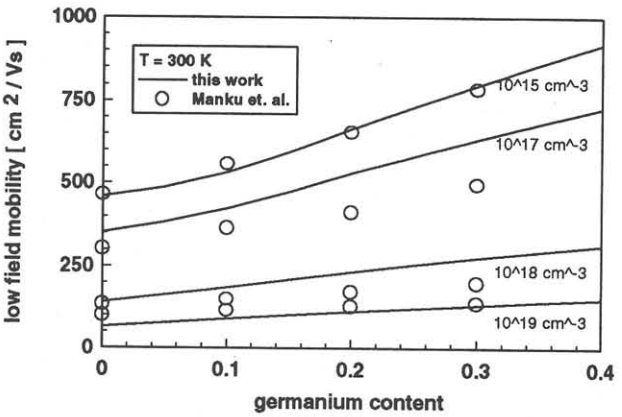

Fig. 3: Dependence of low field mobility from impurity concentration and germanium content of SiGe-layer

4. Results and Discussion

The simulated and experimental saturation currents of transistors with SiGe and boron are compared with simulation and transistors without SiGe and boron in Fig. 4. The data for the silicon transistors were corrected for the threshold voltage shift. The SiGe-MOSFET shows a significant higher current even at a gate voltage of -2.5V, where sheet density in the surface channel is already higher than in the SiGe channel. The comparison shows that the influences of higher mobility and quantum confinement in the SiGe channel are of similar size. We have also calculated the influence of silicon cap layer thickness on threshold voltage and development of a silicon surface channel directly below the gate oxide.

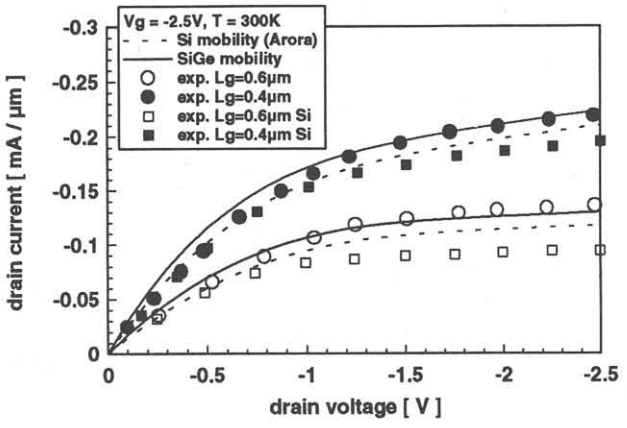

Fig. 4: thick lines: simulation with SiGe mobility model, broken lines: simulation with Si mobility, circles: measurement data of transistor with Si-Ge and boron, squares: measurement data of transistor without SiGe and boron (corrected for threshold voltage shift)

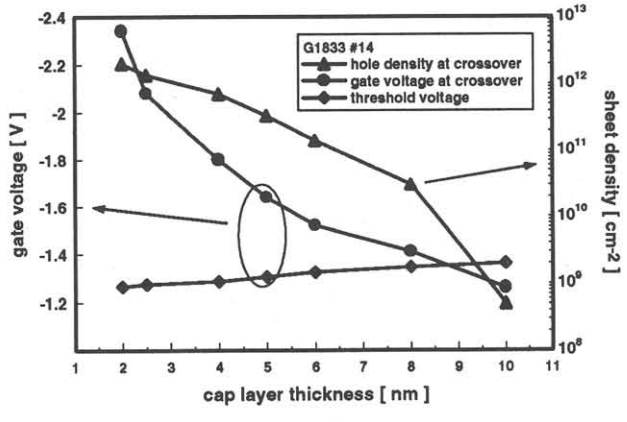

Fig. 5: Simulated influence of cap layer thickness on threshold voltage and the crossover of sheet density in SiGe-channel and surface-channel.

Fig. 5 shows hole density and gate voltages at crossover when the sheet density of the surface channel equals that of the SiGe channel. At gate voltages of about 2V only for cap layers with a thickness below about 3 nm the majority of holes is still in the SiGe quantum well. This is also in agreement with recent calculations of Verdonckt-Vandebroek et. al.[6] Threshold voltage increases linearly with increasing cap layer thickness. Fig. 6 shows that about 150 mV threshold voltage lowering is due to the SiGe channel, which is in good agreement with the bandgap difference for $Si_{0.8}Ge_{0.2}$ of 148mV, while nearly 300 mV result from the boron channel doping.

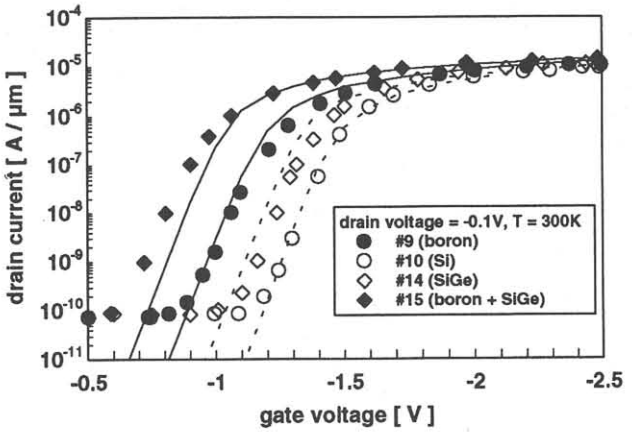

Fig. 6: Threshold voltage shift for 0.6 µm gate length transistors due to different channel profiles - dots: experimental data, lines: simulation

5. Conclusion

We have shown that significantly improved p-channel transistors utilizing a SiGe quantum well for hole transport can be fabricated compatible with standard CMOS technology. For simulation we have developed a mobility model to include the effects of changed effective masses and alloy scattering in a standard device simulator. Our results emphasize the importance of a sufficiently thin cap layer to provide hole transport in the SiGe quantum well at high gate voltages.

Acknowledgement

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