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A Novel Trench Capping Process Using CMP with Endpoint Detection

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Introduction

Recently, oxide-filled deep trenches have drawn greater attention because of their smaller parasitic capacitances and the possibility of reduced stress [1-3]. However, the planarity over the oxide-filled trenches always gets worse because there is no stopper for oxide etch-back, the surface of the as-deposited oxide has dints over the trenches, and the central portion of the oxide in a trench is etched at a higher rate with hydrofluoric-acid-based cleaning. Although the use of reflowed boro-phosphosilicate glass (BPSG) as a trench filler [1] solves the last two problems, the BPSG has to be capped to prevent the out-diffusion of boron or phosphorous, and with the capping process there is still the problem of poor surface planarity.

In order to circumvent the problem, we introduced chemical mechanical polishing (CMP) [4] to planarize the capping oxide over the BPSG in the trench. For the purpose of improving the reproducibility of the CMP, we have developed a novel process featuring a built-in marker for polishing-endpoint detection.

Fabrication Process

First, LOCOS field oxide is formed and deep trenches are etched using a stack of CVD oxide, polysilicon, nitride and field oxide as an etching mask (Fig. 1(a)). The polysilicon serves as a protector against BPSG etch-back and as a built-in marker for polishing-endpoint detection in later processing steps. The nitride, with its small polishing rate, acts as the polishing stopper. Next, the interior of the trench is oxidized, and BPSG is deposited, reflowed and etched back with the underlying CVD oxide. Then, CVD oxide is deposited again to cap the BPSG in the trench (Fig 1(b)). After that, the wafer is polished under the conditions listed in Table 1 until the surface of the nitride appears at level A in Fig. 1 (b). During this step, the motor current to drive the wafer is monitored with an endpoint detector that reflects the frictional characteristics between the polished wafer and the pad. Finally, the remaining polysilicon and nitride are selectively removed and the substrate surface is exposed (Fig.1 (c)).

Results and Discussion

Figure 2 shows the change in motor current during the polishing step. Points A, B and C correspond to the levels of polished surface shown in Fig. 1 (b). For the present combination of slurry and polishing pad, the friction of the polysilicon is larger than that of oxide or nitride, and thus polysilicon on the wafer surface can be detected as rise in current between points B and C. As can be seen in Fig. 2, the signal-to-noise ratio is high enough to judge the polishing endpoint reproducibly.

Figure 3 shows an SEM view of a finished structure corresponding to Fig. 1(c). The surface over the deep trench is very flat while the structure around the LOCOS boundary keeps its original shape. This indicates that the CMP in the present process selectively planarizes the surface over the trench, and the polysilicon and nitride layers effectively protect the active areas.

The above process has been successfully applied to well isolation in deep-submicron CMOS. Figure 4 compares the inter-poly isolation yields over trenches for CMP planarization and for the conventional process, where the trench is filled only with CVD oxide and the surface over the trench is finished by RIE etch-back. The yields are all 100 % for the wafers processed with CMP planarization, whereas the yields for RIE etch-back are less than 60% even if the trench area is selectively over-etched by using additional lithographic and etching steps (relief etch). This indicates the surface over the trench is very flat and there is no crevice or step for poly-etching residue.

Figure 5 shows the dependence of junction leakage current and junction breakdown voltage on the diode perimeter with diode areas kept constant. The designed distance between the edges of diode and trench is only 0.25 μm for the diode with a 0.42-cm perimeter. The other two diodes are completely away from the trenches. Since the data points for the diode adjacent to the trench almost fall on straight lines drawn between the other two points, the presence of deep trenches can be said to have a negligible effect on leakage current and breakdown voltage. This may be attributed to reduced stress around the BPSG-filled trenches.

Conclusions

A novel trench-isolation process has been presented, where deep trenches are filled with BPSG, capped with CVD oxide and planarized by CMP. To improve the reproducibility of the CMP step, a sacrificial polysilicon layer is utilized as a built-in marker for polishing endpoint detection. When applied to well isolation in deep-submicron CMOS, this process results in high inter-poly isolation yield over trenches and a negligible effect on junction leakage and breakdown voltage.

References

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[3] Y. Okazaki, et al., IEEE Trans. Electron Devices, 39 (1992) 2758.
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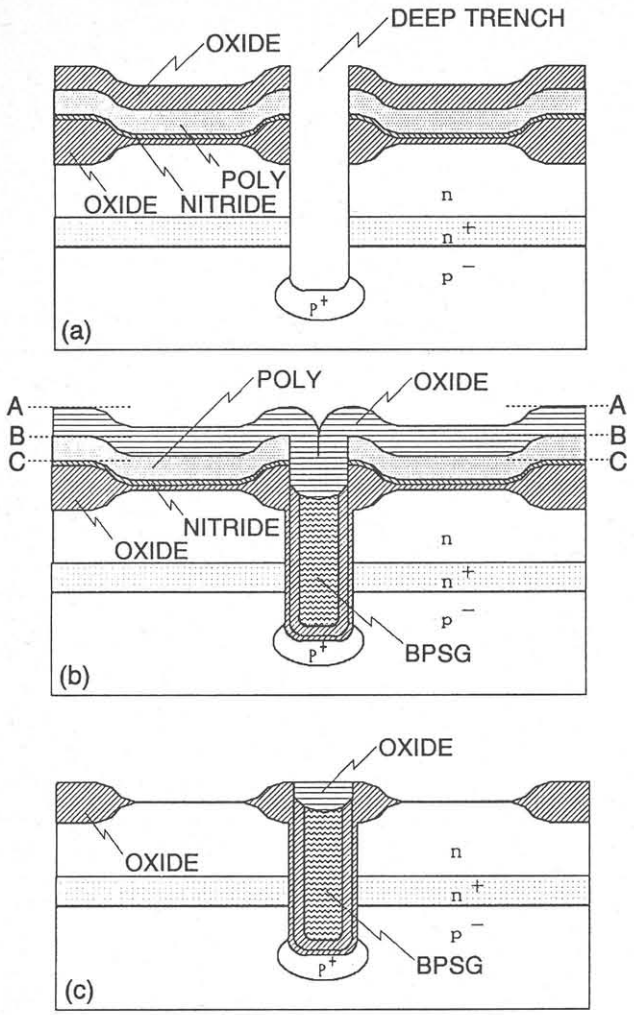

Fig. 1. Processing steps for novel deep-trench isolation.

Table 1. Polishing conditions.

POLISHING PAD	POLYURETHANE IMPREGNATED POLYESTER FELT
SLURRY	AMMONIA-BASED FUMED SILICA
PRESSURE	490 g/cm^2
PAD ROTATIONAL SPEED	32 cm/s
WAFER ROTATION	45 rpm
POLISHING RATE	60 nm/min (CVD OXIDE)

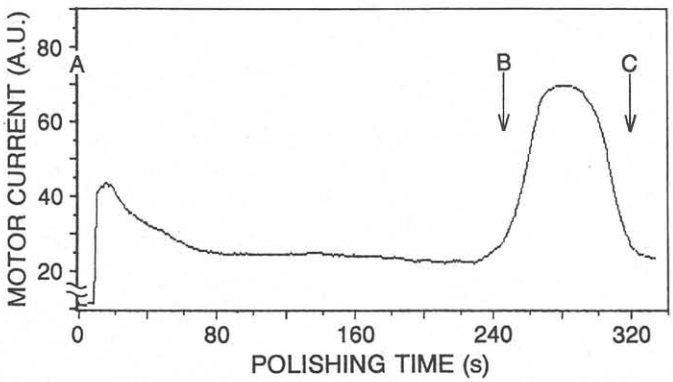

Fig. 2. Change in motor current during the polishing step. Points A, B and C correspond to the levels in Fig. 1 (b).

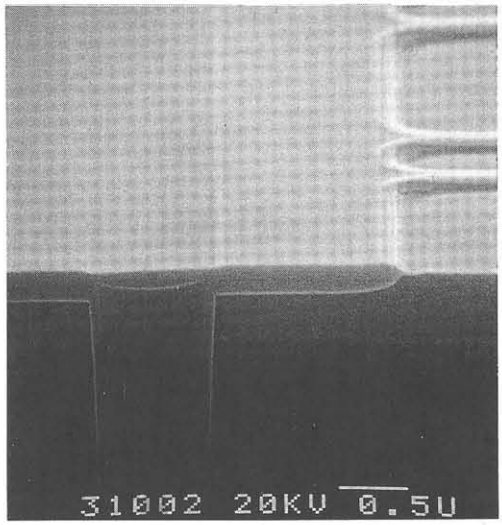

Fig. 3. SEM view of a finished structure corresponding to Fig. 1 (c).

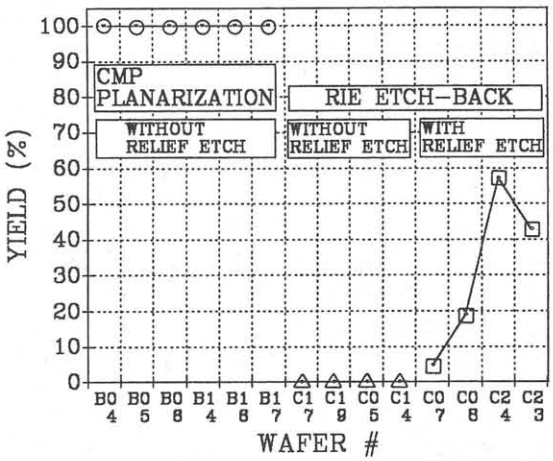

Fig. 4. Inter-poly isolation yields over trenches with a 1.0-μm width and a 4.0-μm pitch. A gate polysilicon interdigital pattern comprising 21 pairs of 78-μm-long, 0.4μm-wide lines with a 2.0-μm pitch was measured.

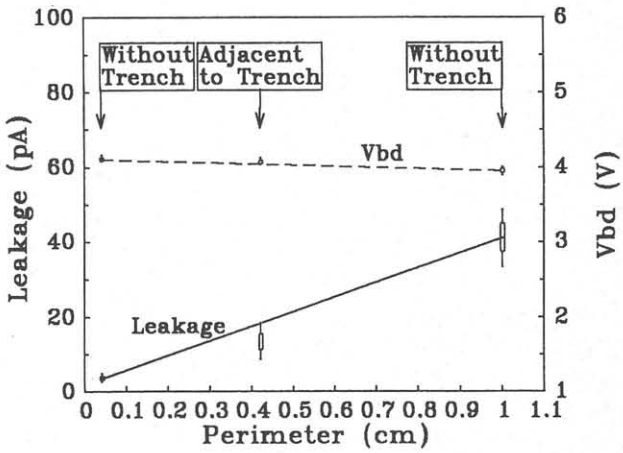

Fig. 5. Leakage currents and breakdown voltages for n^+p junction diodes for different perimeters and structures. Junction area is fixed at 1 X 10^{-4} cm^2, acceptor concentration is 5 X 10^{17} cm^{-3}, and junction depth is 80 nm. Leakage is measured at 3 V and breakdown is defined at 1 nA.