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# High Speed Fully Depleted CMOS/SIMOX Gate Array

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## INTRODUCTION:

Thin film fully depleted SOI ICs have become very attractive for IC application because of their potential advantages such as high speed, high packing density, low power consumption and hard radiation. Gate array is an important branch of custom VLSI. The present paper reports that CMOS/SOI technologies have been developed on thin SIMOX film and applied to gate array ICs.

## FABRICATION PROCESS:

The SIMOX substrate was formed by 170Kev, 1.5E18cm$^{-2}$ oxygen ion implantation and subsequent high temperature annealing at 1300$^{o}$C for 6 hours in an ambient of $N_2$. The natural film doping after processing was estimated at approximately 2E15cm$^{-3}$ n-type. The thickness of surface silicon film of SIMOX material was 180nm.

N-type polysilicon gate self-aligned CMOS technology was developed here. Lateral isolation was achieved by mesa isolation using RIE technology. The process temperature are kept lower than 900$^{o}$C to avoid the degradation of mobility and the quality of gate oxidation The gate oxide was about 30nm in thickness grown by dry thermal oxidation at 900$^{o}$C. Because the fully-depleted submicron devices without source/drain punchthrough are possible even if the channel doping is much small , the threshold voltage was controlled with a relatively lower boron doping of 5.0E16cm$^{-3}$ and phosphorous doping of 2.5E15cm$^{-3}$ for N- and P-channel devices, respectively. The surface silicon film was 140nm thick after processing.

## DEVICE CHARACTERISTICS:

Fig.1 shows the photomicrograph of gate array.

Fig.2 shows the current-voltage characteristics of n- and p-channel SIMOX MOSFET with effective channel length of 1.0um. Both devices have well-behaved characteristics. The Kink effect of NMOSFET is eliminated for fully-depleted SIMOX transisitors. Their threshold voltages are 0.6 and -0.8V, and leakage current are 3.0E-12A/um and 5.0E-12A/um for N- and P-channel devices, respectively.

Fig.3 shows the output waveform of a 19-stage CMOS/SIMOX ring oscillator(L=1um) with a supply voltage of 5V on the gate array. The propagation delay per stage is 243ps. The delay time is smaller than that of non fully-depleted CMOS/SIMOX devices by 30 percent. The higher speed of fully-depleted SOI devices is primarily attributed to the reduction of parasitic capacitance for thin-film SOI structure.

## CONCLUSION:

In conclusion, 1.0um CMOS/SIMOX process has been developed for thin-film fully depleted CMOS gate array ICs. It was proved quantitatively from transistors and ring oscillators that the performance of TFD devices is better than non-FD devices. Using the gate array, a decipherer for space application and a prescaler have been obtained.

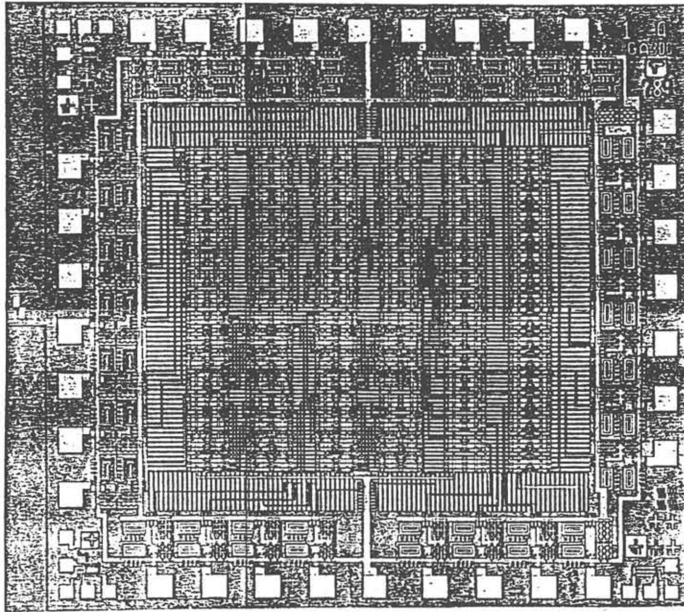

Fig.1 Photomicrograph of CMOS/SIMOX gate array

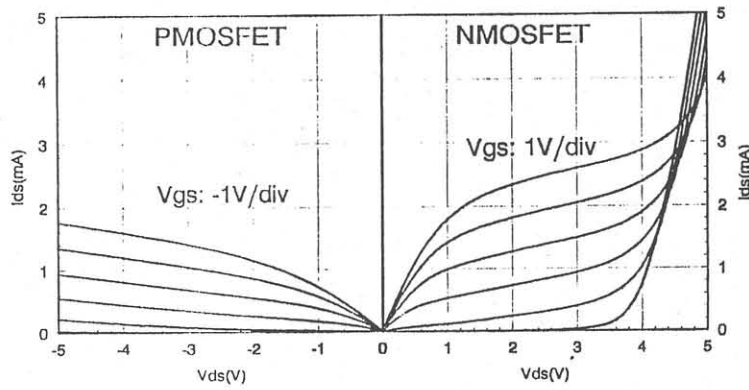


Fig.2 I-V characteristics of SIMOX/SOI MOSFETs($L_{eff}$=1.0um)

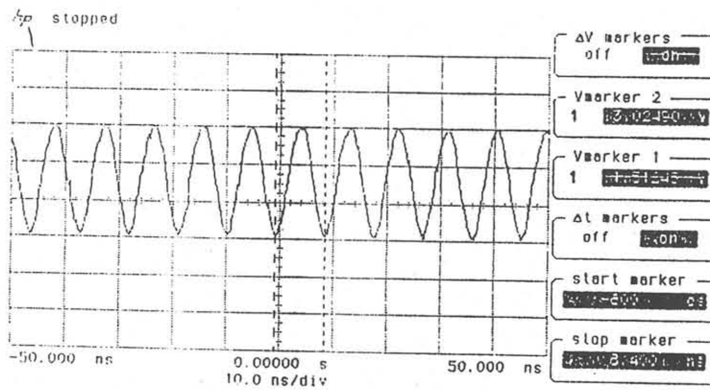


Fig.3 Waveform of a 19-stage CMOS/SIMOX ring oscillator ($L_{eff}$=1.0um, $V_{dd}$=5.0V, Fan in/out=1)