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Low-Temperature Drain Current Characteristics in Sub-10-min-Thick SOI nMOSFET's on SIMOX Substrates

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This paper describes drain current (I_D) characteristics of SOI nMOSFET's with a nominally 8-nm-thick silicon layer and presents a couple of simple analyses. Thin-SOI nMOSFET's were fabricated on SIMOX substrates of (100) Si. They had a 7-nm-thick gate oxide layer, a 90-nm-thick buried oxide layer and a nominal boron doping concentration of $1x10^{17}$ cm^{-3} in the body region[1].

I_D and transconductance (g_m) dependences on gate voltage (V_G) are shown in Fig. 1 for two different temperatures. Figure 1 is for a 0.2-μm gate device. It can be seen that oscillation-like features are superimposed on g_m characteristics at 28 K, although the features were inconspicuous for a long-gate device. It is confirmed that the measurement repeatability is kept during the high/low temperature cycle, which suggests some physical meaning.

We believe a two-dimensional subband system (2DSS) is formed because the silicon layer thickness (t_s) is less than 10 nm in the devices[2]; the energy difference between the lowest subband level and the bottom of the conduction band is 20 meV for t_s = 8 nm. Therefore, it is suggested that the I_D and g_m characteristics are related to the 2DSS since they are observed only at low temperatures less than 100 K (~8meV).

Calculated g_m dependences on V_G for uniform t_s are shown in Fig. 2 for various t_s values. Here, for simplicity, we employed a one-band approximation and assumed a plain rectangular potential well and constant mobility. The calculated g_m curves show small step-like anomalies (indicated by arrows) and are quite different from the experimental results.

Recently, it was shown that the buried oxide surface of high-temperature annealed (100) SIMOX substrates has a rugged square-mosaic 0.4 to 0.8 μm morphology with sloping edges, as shown in Fig. 3, while the superficial silicon layer has a relatively smooth surface[3]. The local t_s deviation is considered to lead to the local deviation of 2DSS[4] and also the local threshold voltage (V_{TH}) deviation [2] because of the energy level deviation in 2DSS. We therefore investigated the origins of those features taking the local t_s deviation into account. The rugged morphology can be modeled as shown in Figs. 4(1) and (2) where (1) is the composition of simple steps divided across the gate width and (2) is that of steps sloping across the gate length that are divided across the gate width. Simulated g_m characteristics are shown for the three different cases - (1) a uniform silicon layer, (2) simple steps, and (3) steps with slopes - in Fig. 5 for L=0.2 μm. The slope angle is assumed to be 1 degree based on AFM observation. For the simple steps, g_m has oscillation-like features. This is because I_D for the each divided MOSFET is a function of both the local V_{TH} and carrier density deviations based on the local-deviated 2DSS. Since each I_D shows sub-linear behavior for the large V_G because of the reduction of $d\phi_s/dV_G$, where ϕ_s is the SOI surface potential, the total g_m has the complicated feature. The nature of this feature becomes very complicated when both the steps and slopes of the buried oxide layer surface are taken into account.

In conclusion, an oscillation-like feature of g_m has been observed in thin-SOI nMOSFET's. It is strongly suggested that the feature is due to the local V_{TH} and carrier density deviations based on the local t_s deviation. All of these are based on the deviation of 2DSS manifested clearly at low temperature.

References

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[4] E. Arnold, Surf. Sci., vol. 58, p. 60, 1976.

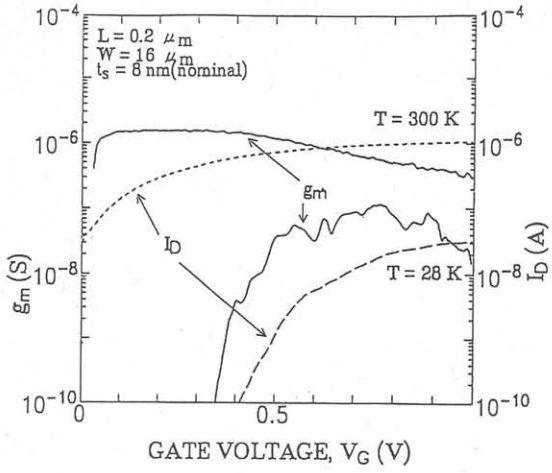


Fig. 1. Experimental results showing I_D and g_m dependences on gate voltage for two different temperatures (28 K and 300 K).

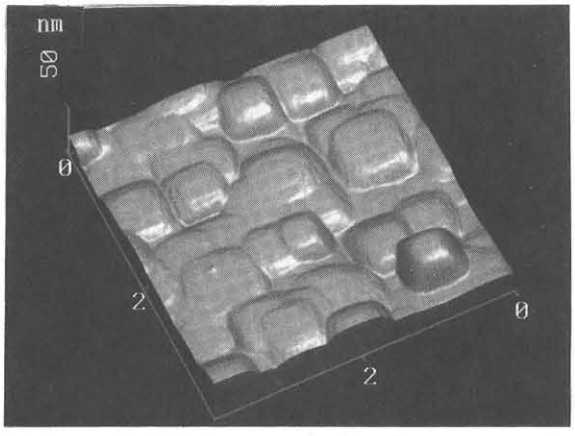
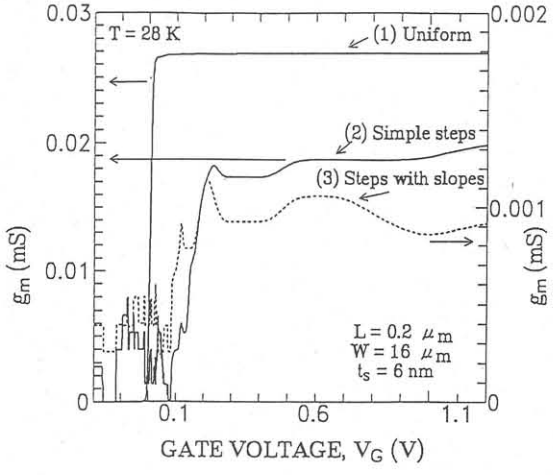


Fig. 3. Surface morphology of a buried oxide layer for the high-temperature annealed SIMOX substrate.
Oxygen dose: 4×10^{17} cm^{-2}.
Annealing temperature: 1350 C.
Annealing time: 4 hours.
Horizontal scale: 2 μm/div.
Vertical scale: 50 nm/div.



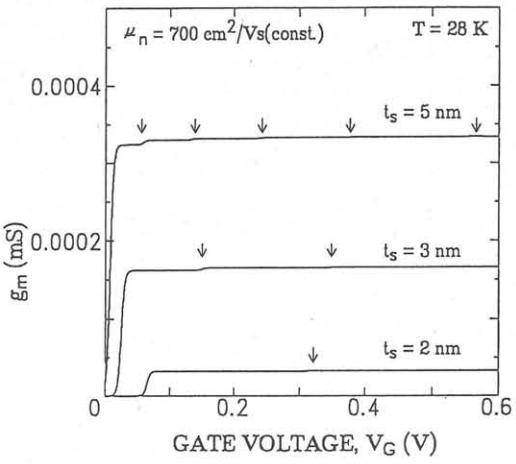


Fig. 2. g_m dependences on gate voltage for three different silicon layer thicknesses. These are simulated results for the uniform t_s case. t_s = 2, 3 and 5 nm.

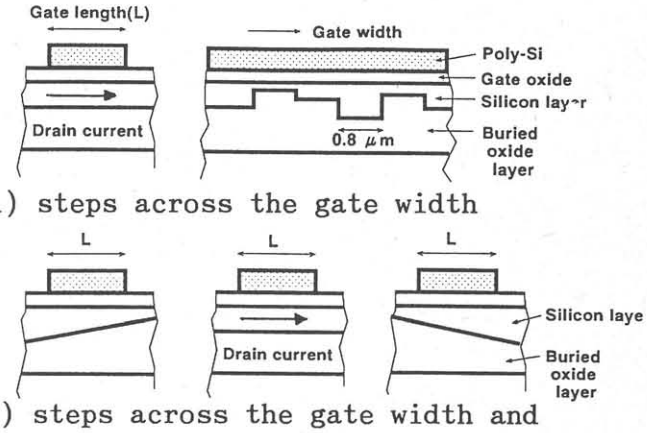


Fig. 4. Simple models for the buried oxide surface morphology.

Fig. 5. g_m dependences on gate voltage for two different silicon layer thicknesses: simulated results for the rugged morphology case. L = 0.2 μm
(1) uniform silicon layer
(2) steps across the gate width
(3) steps across the gate width and slopes across the gate length