

## ON-Current Stability of Poly-Si Thin Film Transistor with Si-rich Oxide as Intermetal Dielectric Film after Negative Bias Temperature Stress

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This paper demonstrates the On-Current ( $I_{on}$ ) stability of poly-Si Thin Film Transistor (TFT) after Negative Bias Temperature (NBT) stress when Si-rich oxide is used as Inter-Metal Dielectrics (IMD) in high-density SRAM employing double-level metal technology. IMD characteristics are compared between conventional TEOS and Si-rich oxide. Fig. 1 shows the schematic cross section of the fabricated poly-Si TFT structure. Spin-On-Glass (SOG) film is deposited for hydrogenation and IMD planarization. Fig. 2 shows the measured drain current ( $I_d$ ) versus gate voltage ( $V_g$ ) curves of p-channel poly-Si TFT at 25°C and 85°C before stress. The stress of -8V is applied to gate for 25,000 sec while drain and source are grounded at 125°C. Fig. 3 compares the  $I_d$ - $V_g$  curves at 85°C before and after stress for 25,000 sec when TEOS (case I) and Si-rich oxide (case II) are used as the IMD. Case II shows little change before and after stress, whereas case I displays  $V_{min}$  increase by about 1V and  $I_{on}$  reduction by more than 1 order. Off current ( $I_{off}$ ) at  $V_g=0V$  has not been changed for both cases.

We also investigated the IMD effect with time passed after the fabrication of TFTs. Fig. 4 displays the normalized change of  $I_{on}$  values after stress for the TFTs with different elapsed time after the fabrication (3 months, 2 months and 10 days). As shown in the figure,  $I_{on}$  after stress in case II is reduced from the initial value by less than 15% independent of the elapsed time. On the other hand, case I shows noticeable decrease rate depending on the elapsed time, which is, larger than 80% decrease and about 20% decrease with stress time in early TFTs and late TFTs, respectively. Furthermore, the early TFTs with only first oxide(USG) passivation shows more serious  $I_{on}$  degradation than those with layered first oxide(USG) and second nitride passivation. As shown in Fig. 5 and 6, the  $I_{on}$  degradation of the early TFTs with TEOS after stress is reflected by the increase of  $V_{min}$  and subthreshold swing(S). It is considered that this phenomenon is closely related to the moisture penetration into the TFT structure from the air with time after fabrication. When TEOS is used for the TFT, the moisture diffuses and reacts with  $SiO_2$  network to make Si-OHs in the gate oxide. The Si-OHs combine with the hydrogen atoms dissociated from Si-H bonds at the interface during the stress, generating both interface traps (increase of S) in the channel and positive oxide charges (increase of  $V_{min}$ ) in the gate oxide<sup>1)</sup>. The increased trap densities in the channel of the early TFTs are calculated by using Levinson's method<sup>2)</sup> as shown in Fig. 7. The trap densities are little increased in case of Si-rich oxide while TEOS shows dramatic increase with stress time.

The stress-immune  $I_{on}$  in the TFTs with Si-rich oxide leads to the stability of  $I_{on}/I_{off}$  ratio in comparison to those with TEOS as shown in Fig. 8. This enables the high density TFT SRAM employing Si-rich oxide as IMD to have robust data retention ability after NBT stress test.

- 1) K. Okuyama, K. Kubota, T. Hashimoto, S. Ikeda and A. Koike, IEDM Tech. Digest (1993) 527.
- 2) J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, J. Appl. Phys. 53 (1982) 1193.

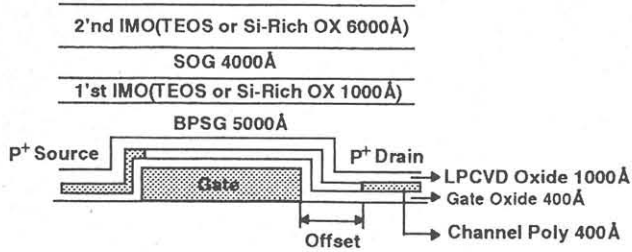


Fig. 1 Schematic illustration of the fabricated poly-Si TFT Structure.

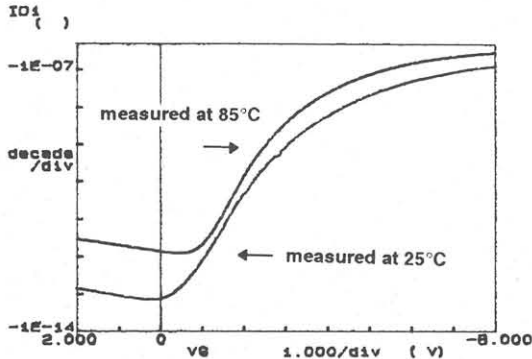


Fig. 2 Drain current versus gate voltage curves of p-channel poly-Si TFT measured at the drain voltage ( $V_d$ ) of -5V before NBT stress.

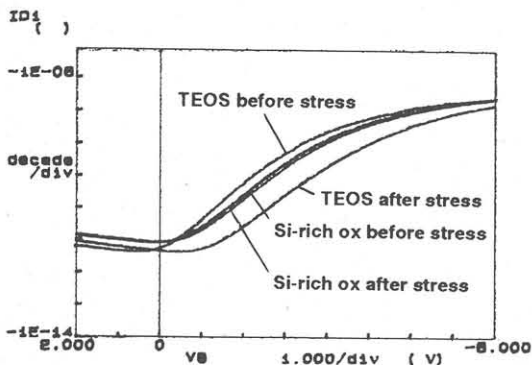
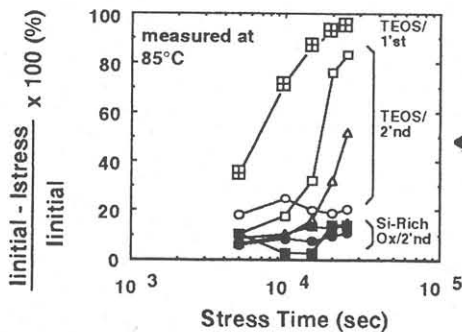


Fig. 3 Drain current versus gate voltage curves of p-channel poly-Si TFT measured at 85°C before and after NBT stress with different IMOs ( $V_d = -5V$ ). In case of Si-rich oxide, the transfer characteristics is little changed after stress.



Period passed after fabrication	IMO/Passivation
□ (filled)	TEOS / 1'st
□ (open)	TEOS / 2'nd
△ (open)	TEOS / 2'nd
○ (open)	TEOS / 2'nd
■ (filled)	Si-Rich Ox./2'nd
▲ (filled)	Si-Rich Ox./2'nd
● (filled)	Si-Rich Ox./2'nd

Fig. 4 On-current ( $I_{on}$ ) change normalized to initial  $I_{on}$  with stress time.  $I_{on}$  is measured at  $V_d = V_g = -5V$ . The table adjacent to the figure shows description for each symbol.

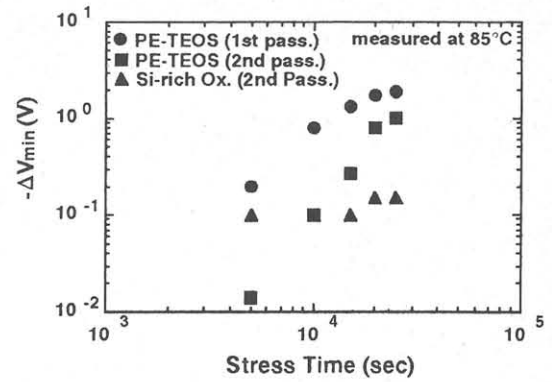


Fig. 5  $V_{min}$  shift with stress time at  $V_d = -5V$  for the early TFTs.

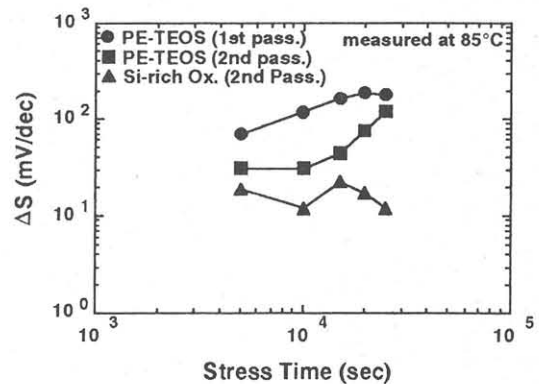


Fig. 6 Shift of subthreshold swing with stress time at  $V_d = -5V$  for the early TFTs.

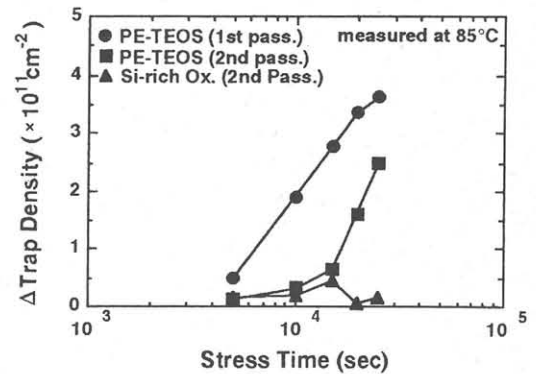


Fig. 7 Change of trap density in the channel of the early TFTs with stress time

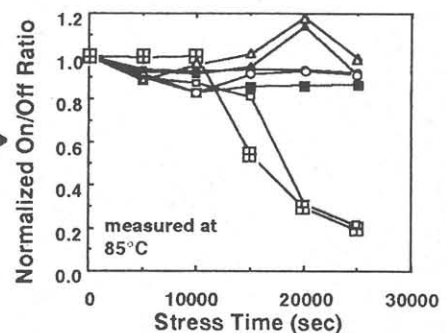


Fig. 8  $I_{on}/I_{off}$  ratio normalized to initial  $I_{on}/I_{off}$  ratio with stress time.  $I_{on}$  and  $I_{off}$  are measured at  $V_g = -5V$  and  $0V$ , respectively. The applied  $V_d$  is -5V for both  $I_{on}$  and  $I_{off}$ . The table adjacent to the figure shows description for each symbol.