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Photovoltaic $Pb_{1-x}Sn_xSe$-on-Si IR-Sensor Arrays for Thermal Imaging

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Photovoltaic infrared sensor arrays fabricated in narrow-gap lead-chalcogenide layers on Si-substrates offer the possibility for low cost infrared focal plane arrays for thermal imaging or spectroscopic applications. Sensitivities of $Pb_{1-x}Sn_xSe$ and related materials are similar to $Hg_{1-x}Cd_xTe$, but processing procedures are much less demanding. This is because the structural quality of even heavily lattice mismatched lead-chalcogenide layers is adequate to fabricate devices with good sensitivities, 2-4 µm thick layers suffice, and because good homogeneity in ternary $Pb_{1-x}Sn_xSe$ for the 8-12 µm wavelength range is much easier to obtain than with $Hg_{1-x}Cd_xTe$ [1-3].

While epitaxy of the narrow gap infrared sensitive materials on lattice matched suitable substrates (like CdZnTe for $Hg_{1-x}Cd_xTe$ sensors) is now common practice, this is not the case for Si-substrates. However, Si-substrates offer significant advantages because of price, size and mechanical properties. A hybrid In-bump-bonding to a Si read-out chip is easy and not limited in size since both the sensor- and readout-chip exhibit the same thermal expansion. In a still more advanced construction, the read-out electronics may be integrated directly into the Si-substrate at locations which are not occupied by sensors. We recently demonstrated such a structure with a lead-chalcogenide sensor array on an active chip [3].

Up to now, we have grown the lead-chalcogenide layers on Si substrates with the help of an intermediate buffer consisting of a ≈200 nm thick stack of BaF_2/CaF_2 in order to get high quality epitaxy, and fabricated sensor arrays in these layers [1,2,4]. However, due to the limited chemical stability of BaF_2, (BaF_2 is soluble in water), standard processing techniques for sensor delineation proofed to be cumbersome. We therefore developed a technique where the MBE-growth is performed on a very thin (5 nm) CaF_2 intermediate epitaxial buffer layer only [3]. This new buffer layer now allows us to use standard photolithographic delineation and wet-etching techniques on full wafers, and we describe here the successful fabrication of such sensor arrays for the first time.

The arrays are fabricated by using the well known blocking Pb-contact technique on p-type $Pb_{1-x}Sn_xSe$ [5]. First, a CaF_2 buffer and then a $Pb_{1-x}Sn_xSe$ layer is grown by MBE onto a Si(111)-wafer. The wafer diameter is presently limited to 3" due to the size of our 2 chamber MBE-equipment. After terminating growth, the blocking Pb-contact is vacuum deposited in the same MBE growth chamber after the sample has cooled down to RT. The wafer is then ex situ overgrown with Ti and Ni for protection of the Pb and better adhesion of the following metal layers, respectively. Sensitive areas are defined by wet-etching the Pb/Ti stack, and Au (which also is used for ohmic contacts) is electroplated on the complete stack. After etching the $Pb_{1-x}Sn_xSe$ layer, a polyimide for insulation of the fan-out is spinned on, patterned and cured. In a last step, Al is vacuum deposited and structured for fan-out. Fig. 1 shows a cross section of such a the device, while a test array consisting of 2x64 sensors with 100 µm and 50 µm pitches and various areas is shown in Fig. 2.

Typical quantum efficiencies of such $Pb_{1-x}Sn_xSe$ sensors are above 50% without antireflection coating. The sensors are diffusion limited down to around

100K, while generation-recombination noise determines the sensitivities below. Fig. 3 shows the distribution of differential resistances at zero bias R_0 (which are inversely proportional to the sensitivity) of a typical $Pb_{1-x}Sn_xSe$ array at 86K. The standard deviation is 11%, 4 sensors are not working due to shorts caused during the fabrication.

We therefore successfully fabricated photovoltaic narrow gap infrared-sensor arrays on Si-substrates using a batch processing technique which entirely relies on simple wet etching techniques and which is suited for full wafer processing.

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[4] J. Masek, T. Hoshino, C. Maissen, H. Zogg, S. Blunier, J. Vermeiren, C. Claeys, Proc. SPIE **1735**, 1992, 54.
[5] H. Holloway, in "Physics of Thin Films", Academic Press, Vol. 11, 1980, pp. 105-203.

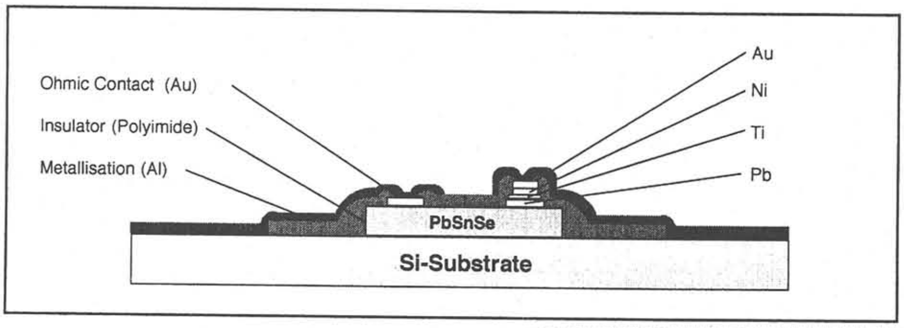

Fig. 1. Cross section of the device lay-out as used for the new fabrication process.

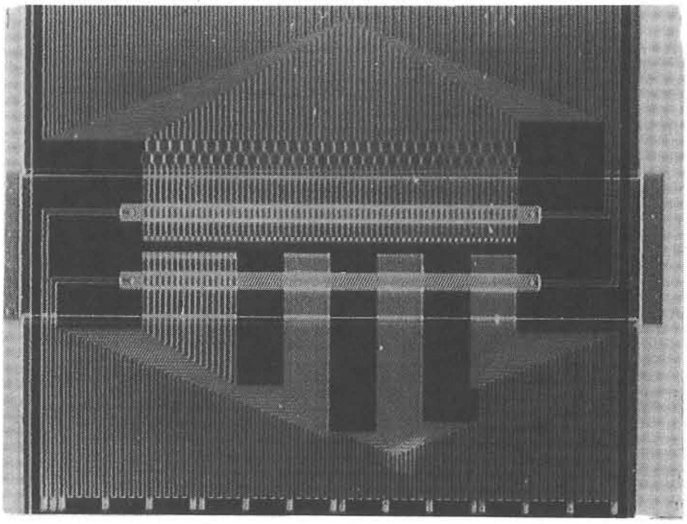

Fig. 2. $Pb_{1-x}Sn_xSe$-on-Si 64x2 test array fabricated with the new batch technique.

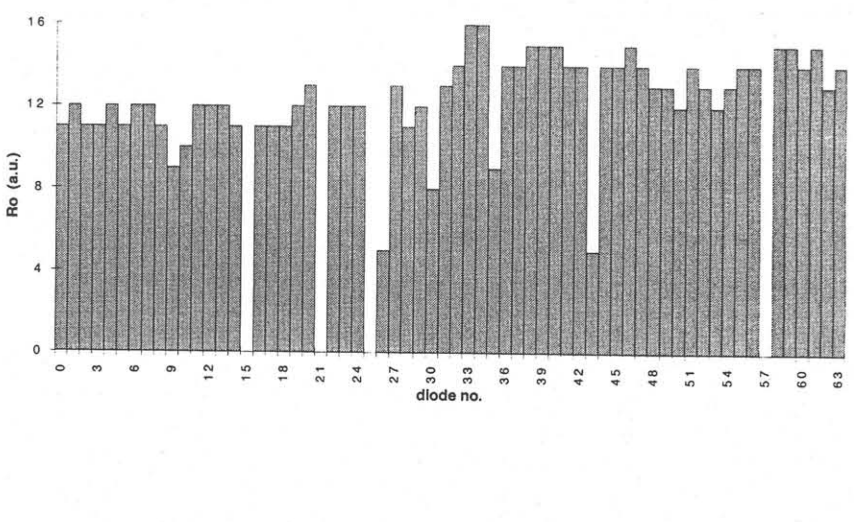

Fig. 3. Distribution of differential resistances at zero bias R_0 for a $Pb_{1-x}Sn_xSe$-on-Si IR-sensor test array with 9 μm cut-off wavelength.