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# A Novel Fabrication Method for Short Channel MOSFET's Using Self-Aligned Ultrashallow Junction Formation by Selective $Si_{1-x}Ge_x$ CVD

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With down-sizing of deep submicron MOSFET's, short channel effects increasingly influence the performance of the devices. The source-drain punch through is an especially crucial problems. Thus, ultrashallow junction formation with control of lateral diffusion of impurities is very important for the progress of ULSI's. The ion implantation method, widely employed in ULSI fabrication, has disadvantages such as the channeling effect and damage introduction to the wafer, and as a result, it is not suitable for fabricating a nm-order shallow junction. In our previous work, we have realized high-performance ultrashallow junction by selective growth of B-doped $Si_{1-x}Ge_x$ on Si using low-temperature ultraclean LPCVD[1]. In this work, a pMOSFET with selective B-doped $Si_{0.5}Ge_{0.5}$ for self-aligned formation of the ultrashallow source/drain regions, schematically shown in Fig. 1(e), has been fabricated and compared with pMOSFET which has source/drain regions fabricated by the conventional B ion implantation.

The MOSFET's were fabricated on the $1.0x10^{15}cm^{-3}$ n-type Si wafers with mirror polished (100) surfaces using self-aligned Si gate process: A 700nm field oxide was formed at 400°C by CVD. A 10nm gate oxide was thermally grown by wet oxidation at 700°C. Then, phosphorus-doped polysilicon was deposited by LPCVD at 600°C and patterned for the gate using ECR plasma etching method(Fig. 1(a)). A thin oxide was formed by wet oxidation at 700°C around the surface of the gate polysilicon and source/drain region(Fig. 1(b)). The oxide thickness of gate surface and source/drain were 37nm and 10nm, respectively, because of the difference in the impurity concentration. Next, oxide of the source/drain regions was removed by wet etching, while the oxide on the gate surface was remained because of the thicker thickness. Then the 15nm-thick B-doped $Si_{0.5}Ge_{0.5}$ ($1.0x10^{20}cm^{-3}$) selective deposition was performed(Fig. 1(d)) on only the source/drain regions by ultraclean LPCVD at 550°C using $SiH_4$, $GeH_4$ and $B_2H_6$ gas system[1] within 1 minute in order to prevent the film deposition on oxide (see in Fig. 2.). For comparison, the source/drain of samples without $Si_{1-x}Ge_x$ was formed by $B^+$-implantation ($1.2x10^{15}cm^{-2}$ at 25keV). Annealing temperature was 700°C for both samples.

The $B^+$-implanted device(gate length is 0.43$\mu$m) clearly shows the punch through characteristics(Fig. 3(a)). On the other hand, the B-doped $Si_{0.5}Ge_{0.5}$ device shows saturation characteristics even for the 0.28$\mu$m device(Fig. 3(b)), and the punch through is observed for only the 0.11$\mu$m device(Fig. 3(c)), although it also shows reduction of current drivability compared with the $B^+$-implanted device, which is due to the sheet resistance of B-doped $Si_{0.5}Ge_{0.5}$. Threshold voltage($V_{TH}$) shift of the B-doped $Si_{0.5}Ge_{0.5}$ device is small compared with the same size $B^+$-implanted device in the region of the gate length below 1.5$\mu$m(Fig. 4). Taking into account lateral distribution of implanted $B^+$ and converting the gate length to the effective gate length, the threshold voltages of the two types of devices can be regarded almost the same. Therefore, lateral extension of source/drain can be negligible and short channel effect is prevented, and as a result the MOSFET with selective B-doped $Si_{0.5}Ge_{0.5}$ in the source/drain regions is suitable for the deep-submicron MOSFET. The high sheet resistance problem of B-doped $Si_{0.5}Ge_{0.5}$ will be solved by the W selective deposition onto the B-doped $Si_{0.5}Ge_{0.5}$. It was recently reported that very short channel nMOSFET was fabricated with shallow source/drain junctions by diffusion from PSG[2]. However, thicker gate sidewalls as a ion implantation mask was necessary to form outside deep source/drain regions. In comparison, the present method has a higher potential to reduce the cell size itself.

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References

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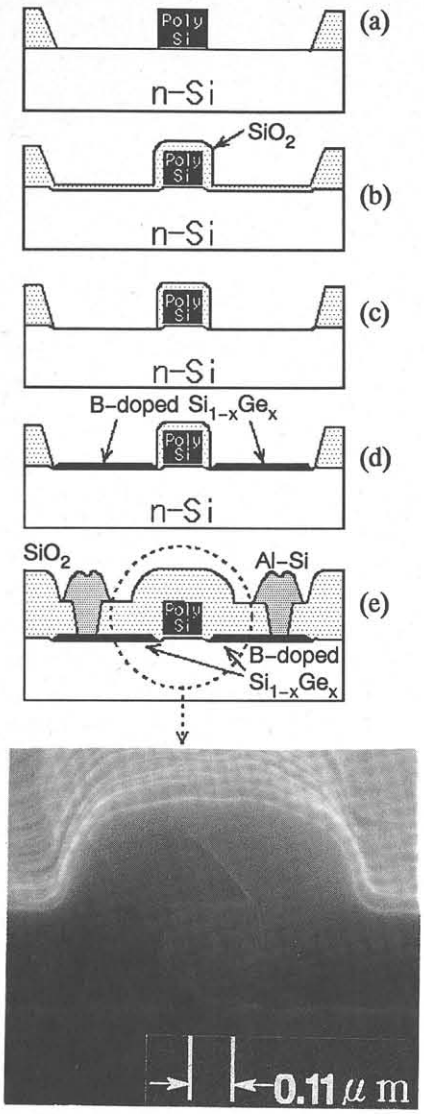


(a) Gate oxidation
Poly Si deposition
Resist patterning
& ECR etching
Oxide removal

(b) Oxidation

(c) Oxide removal of source/drain regions by wet etching

(d) Selective deposition of B-doped $Si_{1-x}Ge_x$

(e) Passivation & metallization

The rough surface in the source/drain regions results from island growth of B-doped $Si_{0.5}Ge_{0.5}$.

**Fig. 1.** Fabrication process of pMOSFET with selective B-doped $Si_{1-x}Ge_x$ in the source/drain regions.

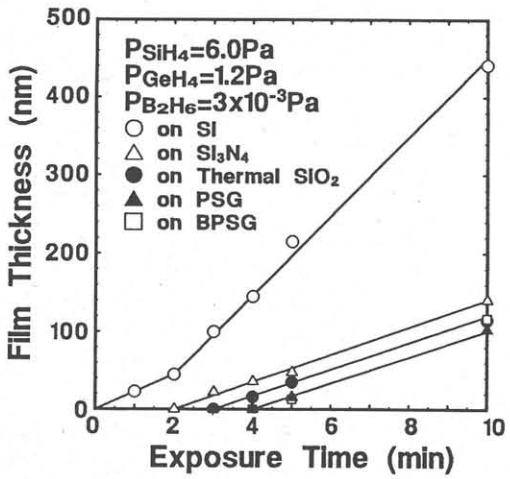


**Fig. 2.** Deposition time dependence of B-doped $Si_{0.5}Ge_{0.5}$ film thickness on Si for various mask film materials.

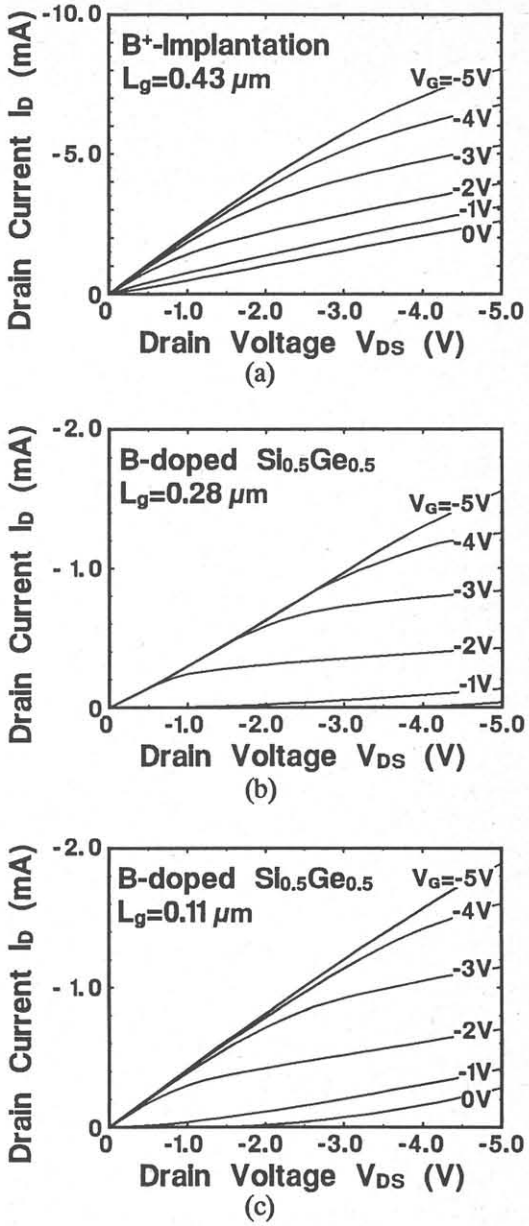


**Fig. 3.** $I_D$–$V_{DS}$ characteristics of (a)0.43$\mu$m $B^+$-implanted device, (b)0.28$\mu$m and (c)0.11$\mu$m B-doped $Si_{0.5}Ge_{0.5}$ devices.

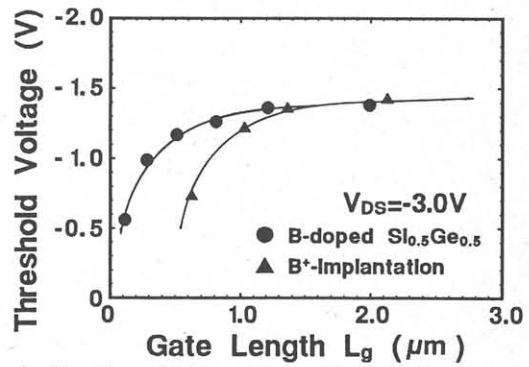


**Fig. 4.** Gate length dependence of threshold voltage of B-doped $Si_{0.5}Ge_{0.5}$ device and $B^+$-implanted device.