Fabrication and Evaluation of Three-Dimensional Optically-Coupled Common Memory

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1. Introduction
A three-dimensional optically-coupled common memory (3D-OCC memory) is an intelligent memory for high-speed parallel processing, in which vertically stacked memory layers are mutually interconnected by optical coupling with GaAs LED/photodetector pairs. Very-high data transfer speed (128Gbits/sec) has been demonstrated by simulation for a 4 layer 3D-OCC memory[1]. In this paper, we have for the first time demonstrated the operation of the 3D-OCC memory test chip on which GaAs LEDs are integrated and confirmed the optical writing operations.

2. Concept of 3D-OCC Memory
The 3D-OCC memory cell circuit has two LEDs and two photodiodes (PDs) for optical coupling as shown in Fig.1. This flip-flop circuit consists of the data store portion with PDs and the data transfer portion with LEDs. The memory layers are vertically stacked with face to face configuration of LED and PD pairs. The data transfer is performed through the optically coupled flip-flops[2,3].

3. Fabrication of 3D-OCC Memory
The 3D-OCC memory test chips were fabricated using 2μm CMOS technology. SEM micrographs of a fabricated 3D-OCC cell circuit are shown in Fig.2, where the LEDs are located just above the PDs. Since the size of GaAs LEDs used here is relatively big (~50μm square) and the LED overlaps both of the underlying PDs, the surface of PD2 was masked by an Al overlayer to guarantee the incidence of the LED light to PD1. Figure 3 shows process sequence for hybrid integration of LEDs on a Si chip[4]. A GaAs LED wafer was thinned to about 120μm by polishing the back side of the substrate. Each LED was isolated with a required size by mesa etching after formation of the ring electrodes for microbonding and the mesh electrodes for back electrodes of LEDs. These LED chips were bonded on the PIQ layer coated above the photodiodes in the optically coupled flip-flop circuit with an alignment accuracy of 1μm using the micrometal (In/Au) bumps. A newly developed three-dimensional wafer aligner was used for the microbonding of LEDs.

4. Evaluation of Test Chip
The operation waveforms measured for a 3D-OCC memory test chip are shown in Fig.4, where the electrical writing/reading operation for the data "0" is executed in the first two cycles and the optical writing/electrical reading operation in the latter two cycles. In the optical writing/electrical reading operation, the data "0" is optically written after the electrical writing of the data "1". In other words, the electrically written data "1" is optically re-written by the data "0" in the former cycle of the latter two cycles. As is obvious from the output waveform in the figure, this optically re-written data "0" is correctly read-out. Also, the output waveforms for the electrical writing/reading operation in the first two cycles are shown for the comparison. It is clear that the electrical writing/reading operation for the data of "0" and "1" is correctly performed. This indicates that the test circuit operates correctly and hence the measured result for the optical writing/electrical reading operation is correct. Thus, we have confirmed the basic function of 3D-OCC memory test chip.

5. Summary
3D-OCC memory test chips have been fabricated for the first time using 2μm CMOS technology. The optical writing operation in the 3D-OCC memory has been successfully demonstrated.
References


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Fig.1 Memory cell circuit with photodiodes PD1 and PD2 and light emitters LED1 and LED2.

Fig.2 SEM photographs of fabricated 3D-OCC memory test chip before (a) and after hybrid integration of GaAs LEDs (b).

Fig.3 Process sequence for hybrid integration of LEDs on a Si chip.

Fig.4 Measured operation waveforms in a 3D-OCC memory test chip.