Extended Abstracts of the 1994 International Conference on Solid State Devices and Materials, Yokohama, 1994, pp. 971-972



# A Novel Wire Transistor Structure with In-Plane Gate Using Direct Schottky Contacts to 2DEG

H. Okada[1], K. Jinushi[1], N.-J. Wu[1], T. Hashizume[1] and H. Hasegawa[1,2]

[1]*Department of Electrical Engineering, Hokkaido University, Sapporo 060, Japan*
[2]*Research Center for Interface Quantum Electronics, Hokkaido University, Sapporo 060, Japan*

Fine semiconductor wire structures having extremely high electron mobility are attractive for applications to future devices in quantum regime. For realization of wire structures with desired perfection and quality, suitable fabrication methods of damage-free structures are required. Special growth techniques such as preferential growth technique and growth-cleavage-regrowth technique have been used to realize burried wires and edge quantum wires. However, they do not seem to be suitable for large scale planer integration. On the other hand, the wire transistors based on electrical control of the depletion width are very simple, and have potential use for many electronic devices and LSIs.

The purpose of this paper is to propose and fabricate a novel wire transistor structure with in-plane gate using direct Schottky contacts to AlGaAs/GaAs quantum well (QW). The novel wire transistor structure is shown in Fig.1, where the effective width of the wire is modulated by the change of the width of quasi-planer depletion layer with bias. It is shown in this paper that the novel structure can be realized by a combination of the electron beam (EB) lithography and the in-situ selective electrochemical technology which we have recently shown[1,2] to be capable of forming a direct Schottky contacts to QWs with two dimensional electron gas (2DEG).

Figure 2 shows the molecular beam epitaxy (MBE) grown QW structure with the electron sheet carrier density, $n_s$, of $1.4\times10^{12}cm^{-2}$ and mobility of $32000cm^2/Vs$ at 77K. The SEM image and corresponding schematic view of the wire transistor structure are shown in Fig 3. Rectangular bar with vertical side walls were fabricated by the EB lithography and wet chemical etching. The width of the bar, $W_B$, was 0.5-2$\mu$m. The side walls were slightly etched by anodic dissolution prior to the in-situ pulse plating of Pt in the same electrolyte. Selective and direct contact formation to the QW edge becomes possible by taking advantage of the fact that both *in-situ* electrolytic etching and metal plating take place selectively at the place with the lowest potential on the surface, i.e., the QW part.

Figure 4 shows the measured current-voltage characteristics of a device with $W_B=2\mu m$. The current was found to be linearly modulated by the side gate voltage, Vs, reflecting control of the width of the depletion layer.

In order to make quantitative comparison with experiments, a theory on transistor characteristics was developed, paying attention to the depletion behavior of the quasi-planer depletion layer.[3] Depletion properties were also directly studied experimentally by electron beam induced current (EBIC) technique on a simple Schottky/2DEG diodes.[4] Figure 5 shows the calculated transistor characteristics based on the depletion theory with measured sheet carrier concentration and mobility of 2DEG in QW. From Figs. 4 and 5, it is seen that theory and experiment are in excellent agreement.

In summary, We have proposed a novel wire transistor structure with in-plane gate and the feasibility of its fabrication by a combination of the electron beam lithography and the selective electrochemical technology. The observed transistor characteristics, although they are not optimized, are in excellent with theory on the depletion characteristics of quasi-planer depletion layer. The precise width control with low capacitance may lead to a new class of quantum devices.

[1] N.-J. Wu, T. Hashizume and H. Hasegawa: SSDM'93, Jpn. J. Appl. Phys. **33**(1994) 936.
[2] T. Hashizume, G. Schweeger, N.-J. Wu and H. Hasegawa: to be published in J. Vac. Sci. Technol. B (1994), July/August issue.
[3] B. Gelmont, M. Shur and C. Moglestue: IEEE Trans. **ED-39**(1992) 1216.
[4] T. Hashizume et al.:"C-V and EBIC study of direct Schottky contacts to quantum wells formed by in-situ selective electrochemical process", to be presented at SSDM'94.

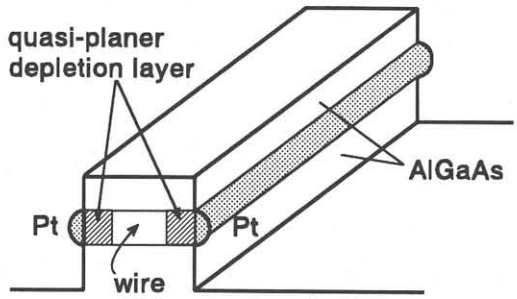
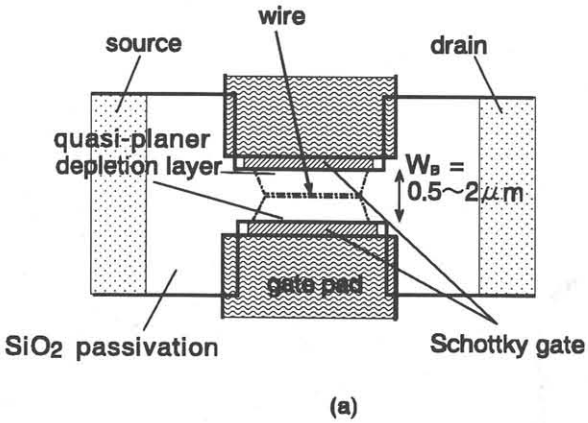


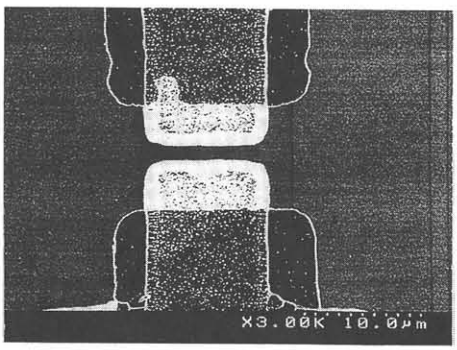

Fig.1. Schematic illustration of selective plated Pt to the QW edge.

| | | |
|---|---|---|
| GaAs cap | $1x10^{18}cm^{-3}$ | 50Å |
| $Al_{0.3}Ga_{0.7}As$ | undoped | 500Å |
| Si $\delta$-doping | $5x10^{12}cm^{-2}$ | —— |
| $Al_{0.3}Ga_{0.7}As$ | undoped | 50Å |
| GaAs QW | undoped | 200Å |
| $Al_{0.3}Ga_{0.7}As$ | undoped | 1000Å |
| GaAs buffer | undoped | 5000Å |
| SI GaAs substrate | | |

Fig.2. GaAs/AlGaAs QW structure grown by MBE.




(a)




(b)

Fig.3. (a)Schematic view and (b)SEM image of the wire transistor structure with the Schottky barriers at the edge of the QW layer.

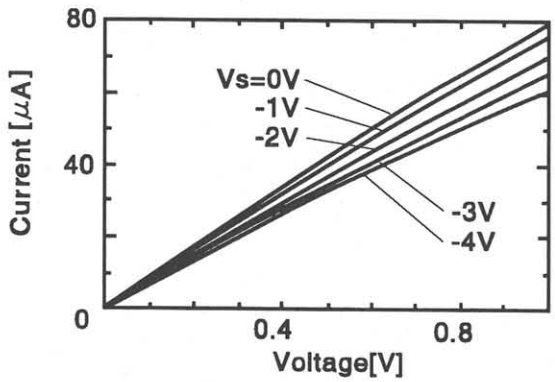



Fig.4. Current-voltage characteristics of the 2$\mu$m wide wire for various side gate voltages,Vs.

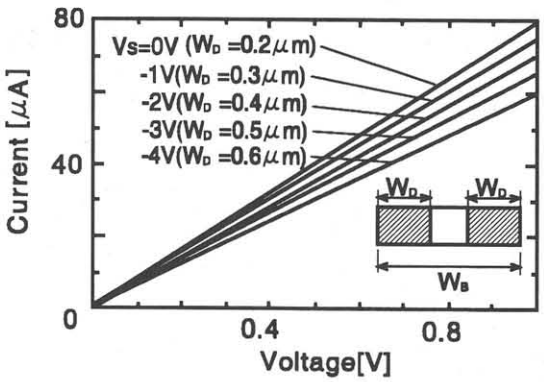



Fig.5. Calculated I-V characteristics based on the depletion theory on the quasi-planer depeletion layer.