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InAs Field-Effect Transistors with a Deep Quantum Well Structure

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Device characteristics of FETs using an InAs/AlGaAsSb deep quantum well structure (InAs DQW FETs) was studied for the first time. The InAs DQW FET with 1μm gate length (L_g) showed good pinch-off property, high transconductance of 450mS/mm and $f_T \cdot L_g$ product as high as 30GHz•μm.

The InAs DQW FET structure was schematically shown in FIG.1. InAs/AlGaAsSb DQWs have extremely large conduction band offset and electrons are effectively confined to the well. All layers were grown on GaAs substrate using conventional MBE technique. Following to GaAs buffer layer, highly resistive $Al_{0.8}Ga_{0.2}As_{0.15}Sb_{0.85}$ buffer/lower barrier layer of 600nm, InAs channel of 15nm, $Al_{0.8}Ga_{0.2}As_{0.15}Sb_{0.85}$ upper barrier layer of 35 nm and InAs cap layer of 2 nm were grown sequentially. AlGaAsSb buffer/barrier layer is lattice-matched to InAs, which was confirmed by XRD. In order to control the composition of Sb and As of the AlGaAsSb layer to realize lattice-matching to InAs, As/Sb pressure ratio was strictly set to be 40. Without any intentional doping, typical electron mobility of the wafer was 15,000cm^2/V•sec and sheet electron density was $1.5x10^{12}/cm^2$. Note that, though there exists large lattice-mismatch of 7% between InAs and GaAs substrate and AlGaAsSb buffer layer thickness is relatively small, electron mobility mentioned above was superb. Part of this is due to the specific substrate temperature profile we employed during the growth [1].

Device fabrication with non-alloyed ohmic electrodes was carried out as follows. First, layers were etched down to GaAs substrate using H_3PO_4 mixture etchant for the channel isolation. Gate electrode of 400nm Al was formed by ordinary lift-off process. To fabricate non-alloyed ohmic electrodes, selective etching of AlGaAsSb over InAs was done and AuGe/Ni/Au was evaporated directly onto InAs layer. The resultant contact resistance was as small as 0.02Ω mm.

The I-V characteristics of thus fabricated InAs DQW FET (L_g=1μm) is shown in FIG.2. Though relatively high drain-conductance was observed, transconductance was 450mS/mm. The gate leakage current was several tens of μA. The cutoff frequency was measured for the devices with L_g ranging from 1 to 2μm. The result is shown in FIG.3. Observed f_T vs L_g relationship shows that $f_T \cdot L_g$ product is as high as 30GHz•μm at V_{ds}=0.9V and V_g=-0.4V.

Our primary research of InAs DQW FETs resulted in the effective electron velocity of $1.9x10^7$cm/sec, which is higher than those of conventional and pseudomorphic HEMTs and approaching that of InGaAs HEMT on InP substrate. We believe that, with some improvements of device structure such as introducing gate recess structure and optimal spacing between electrodes, superior device performance of InAs DQW FETs would be revealed.

[1] N.Kuze et al, Proc. 8th International Conference on Molecular Beam Epitaxy (to be published), 1994

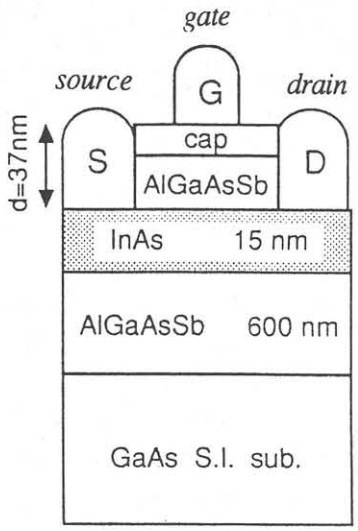

FIG.1 Schematics of the InAs DQW FET.
Ohmic electrodes were directly evaporated onto InAs layer.
Separation between source and drain was set to be 5μm.

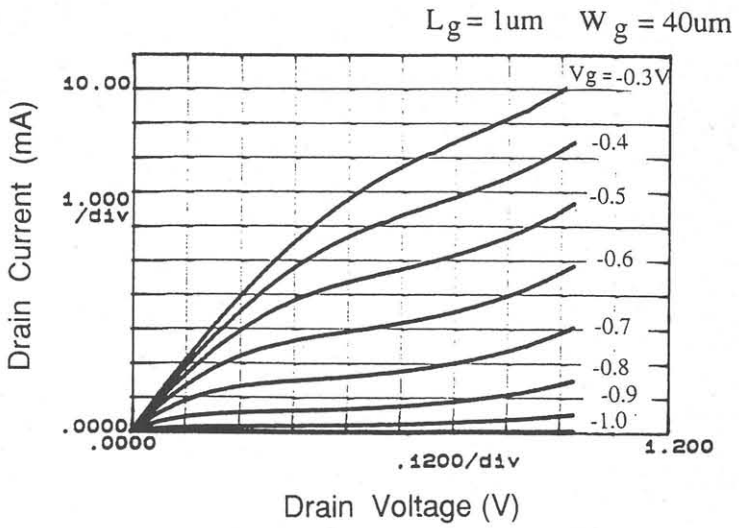

FIG.2 I-V measurement of the device. Drain current was well pinch-offed with the gate bias of -1.0V and the maximum transconductance was 450mS/mm.

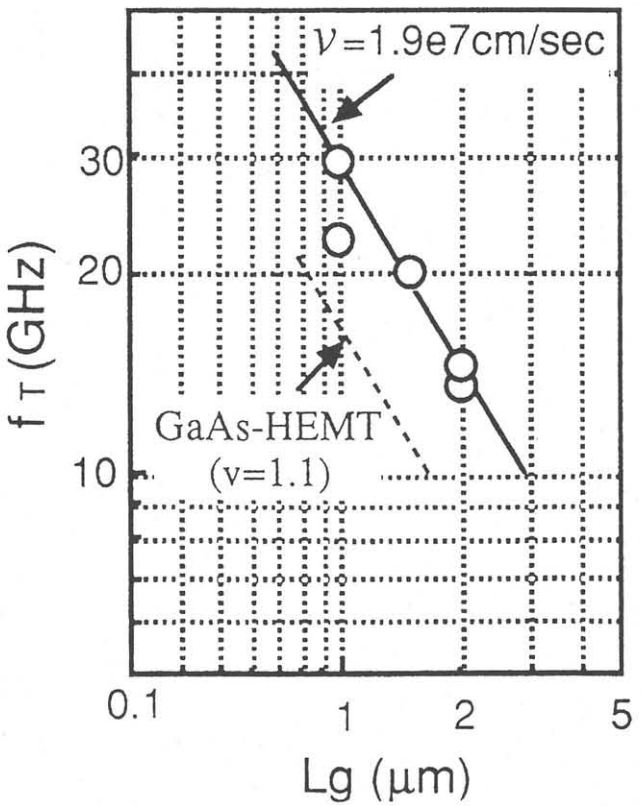

FIG.3 Summary of microwave measurements of the devices. Effective electron velocity more than 1.9×10^7cm/sec was indicated.